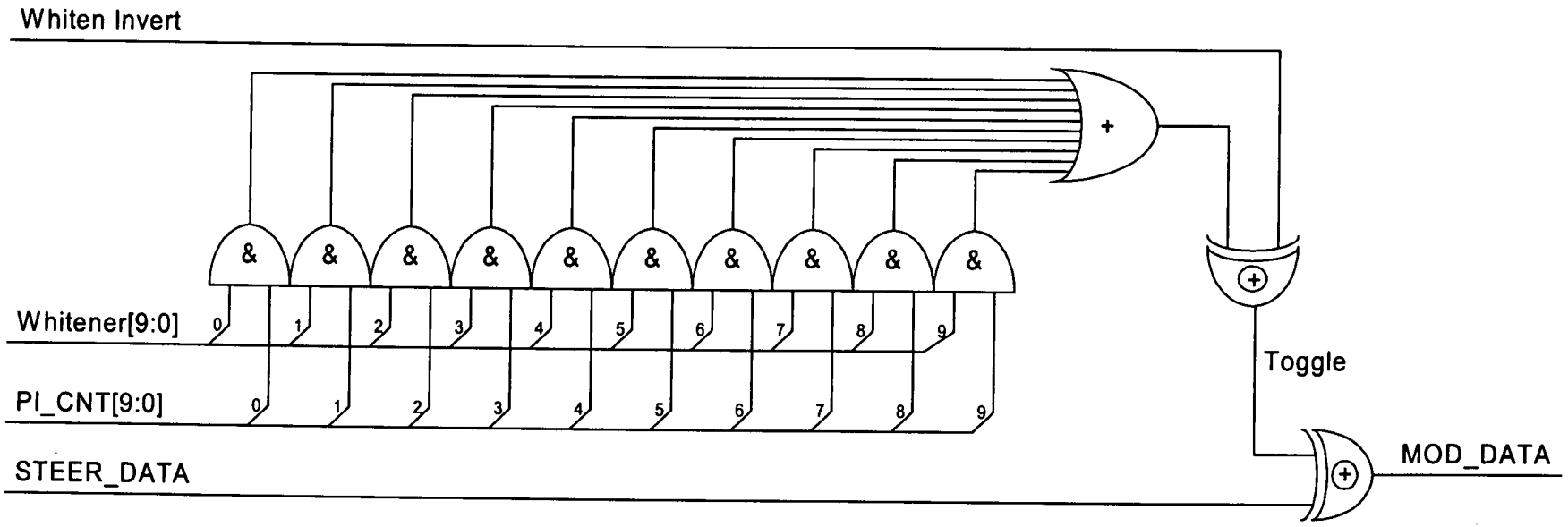

Whiten Invert
+
&
&
&
&
&
&
&
&
&
&
Whitener[9:0]
0
1
2
3
4
5
6
7
8
9
PI_CNT[9:0]
0
1
2
3
4
5
6
7
8
9
Toggle
STEER_DATA
MOD_DATA

FIG. 28

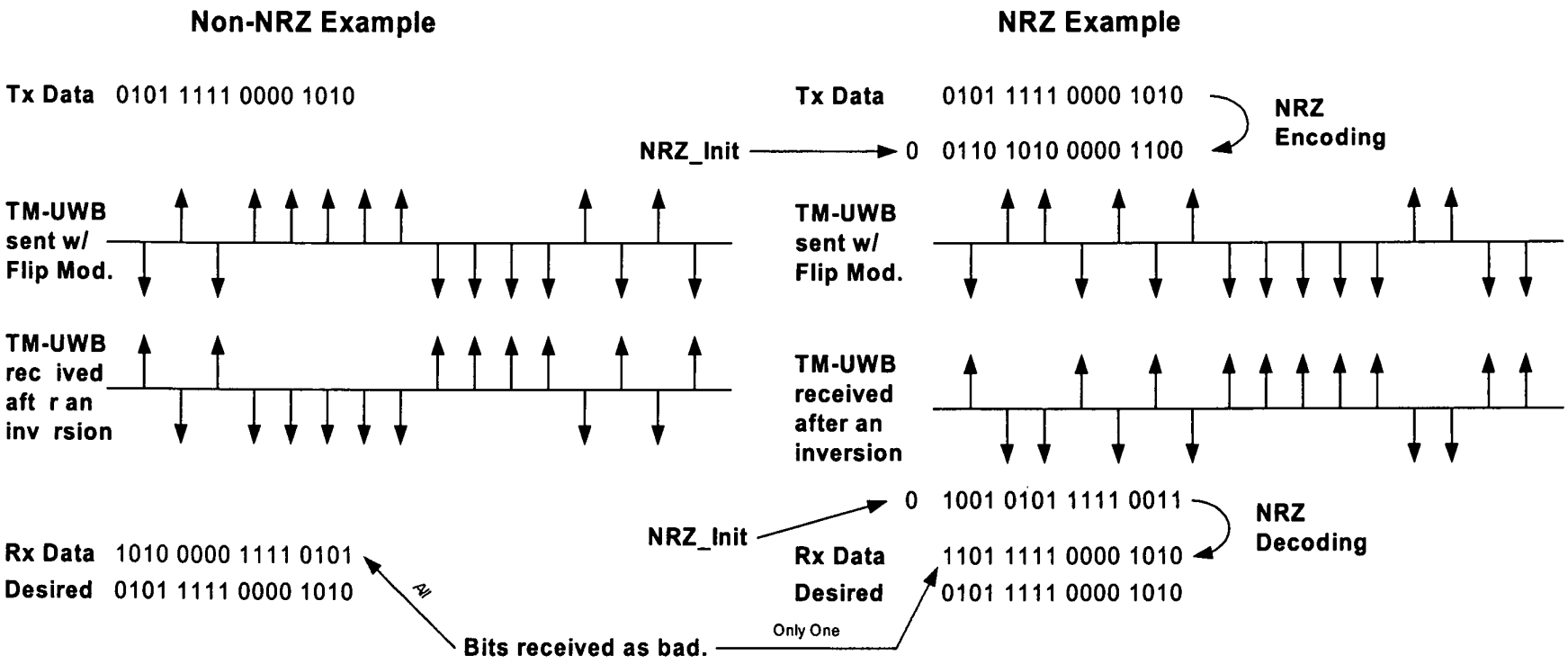

Non-NRZ Example
Tx Data 0101 1111 0000 1010
TM-UWB sent w/ Flip Mod.
TM-UWB rec ived aft r an inv rsion
Rx Data 1010 0000 1111 0101
Desired 0101 1111 0000 1010
All
Bits received as bad.
NRZ Example
Tx Data 0101 1111 0000 1010
NRZ Encoding
NRZ_Init
0 0110 1010 0000 1100
TM-UWB sent w/ Flip Mod.
TM-UWB received after an inversion
0 1001 0101 1111 0011
NRZ_Init
NRZ Decoding
Rx Data 1101 1111 0000 1010
Desired 0101 1111 0000 1010
Only One

FIG. 29

Timer Control Logic
Simplified Block Diagram

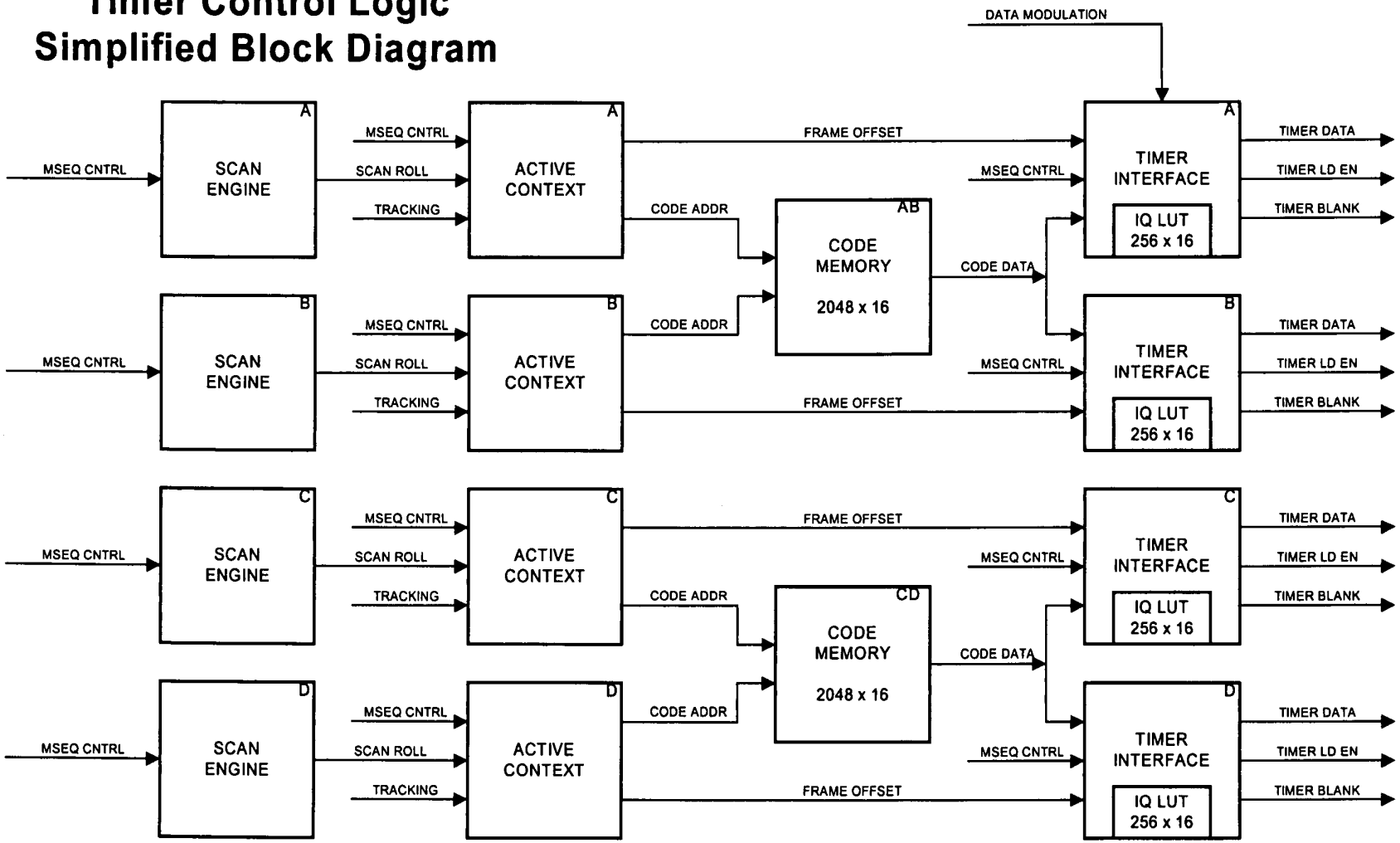


FIG. 30

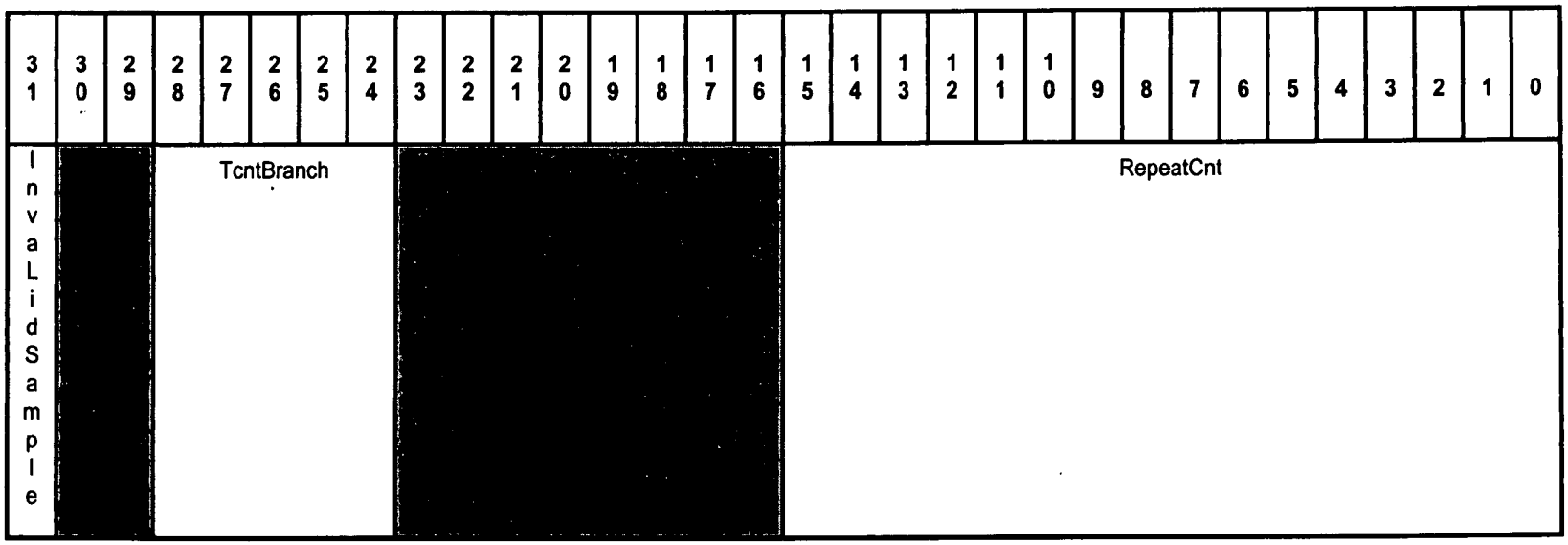

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
InvalidSample
TcntBranch
RepeatCnt

FIG. 31

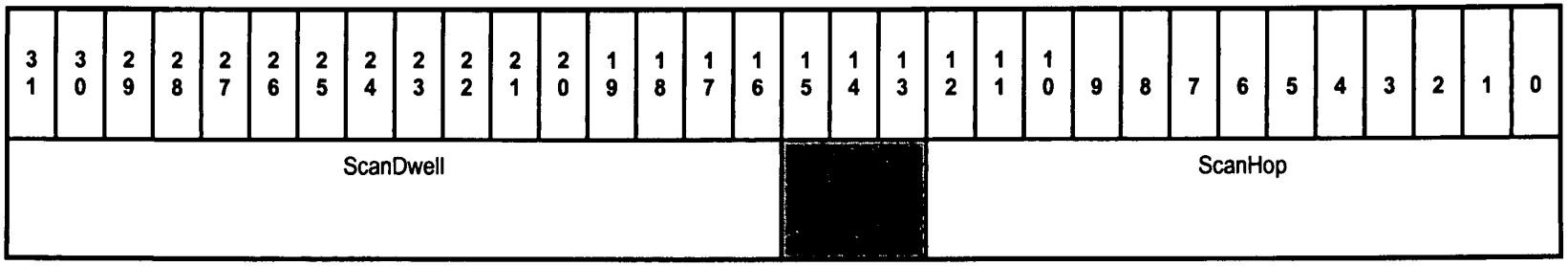

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ScanDwell
ScanHop

FIG. 32

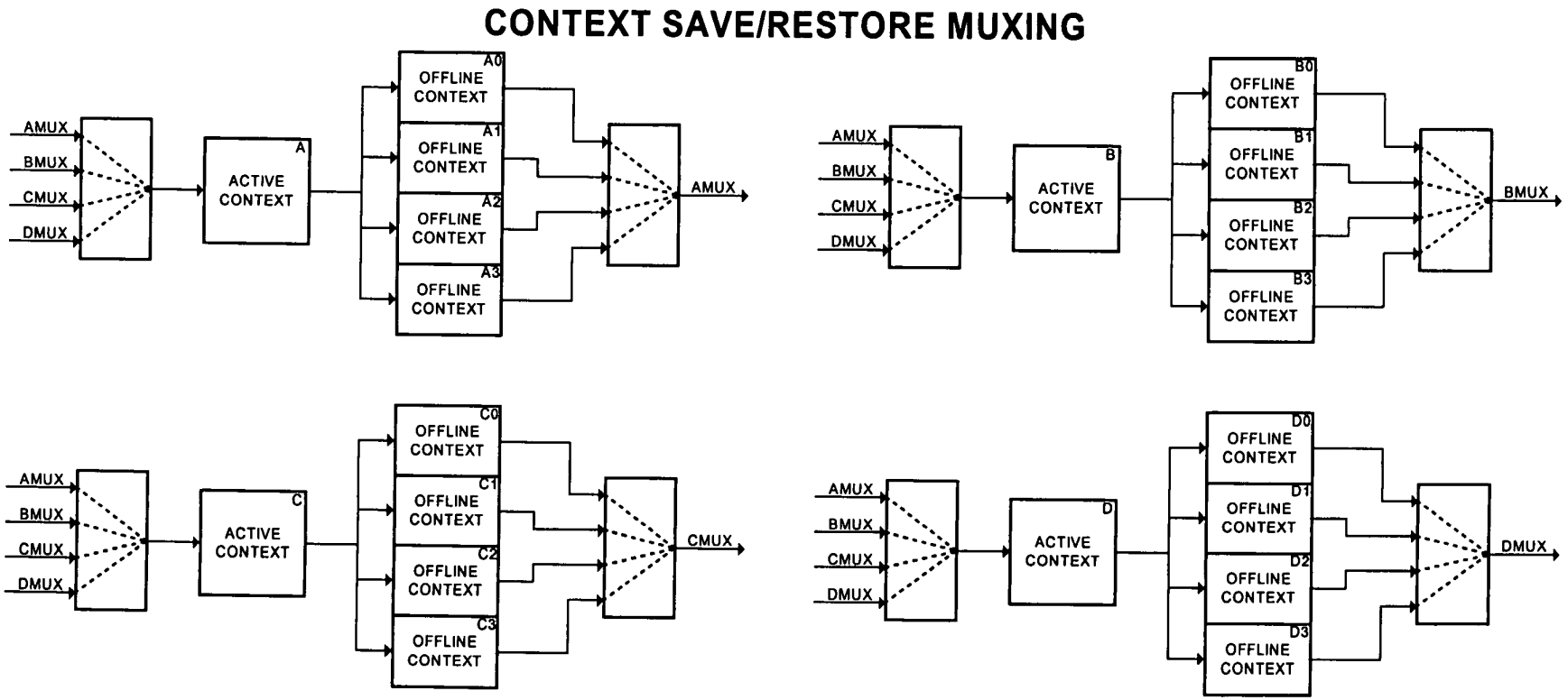

CONTEXT SAVE/RESTORE MUXING
AMUX
BMUX
CMUX
DMUX
ACTIVE CONTEXT
A
OFFLINE CONTEXT
A0
A1
A2
A3
AMUX
ACTIVE CONTEXT
B
OFFLINE CONTEXT
B0
B1
B2
B3
BMUX
ACTIVE CONTEXT
C
OFFLINE CONTEXT
C0
C1
C2
C3
CMUX
ACTIVE CONTEXT
D
OFFLINE CONTEXT
D0
D1
D2
D3
DMUX

FIG. 33

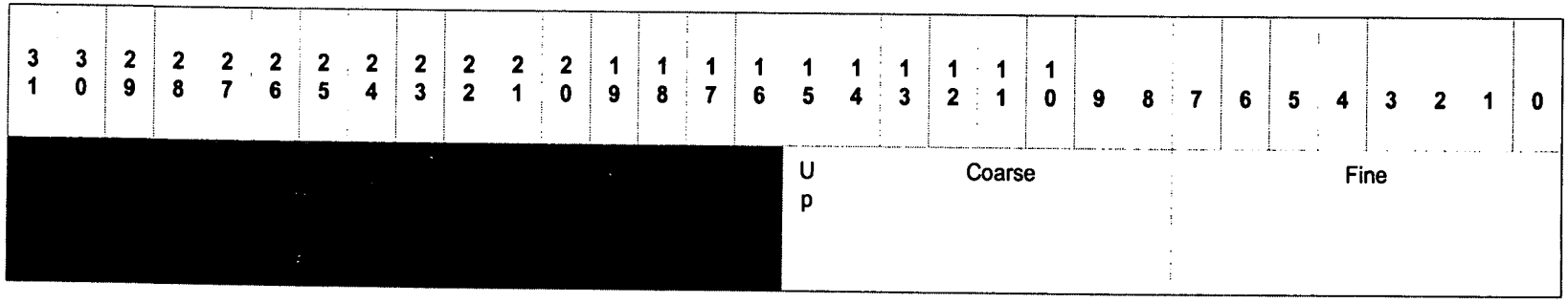

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Up
Coarse
Fine

FIG. 34

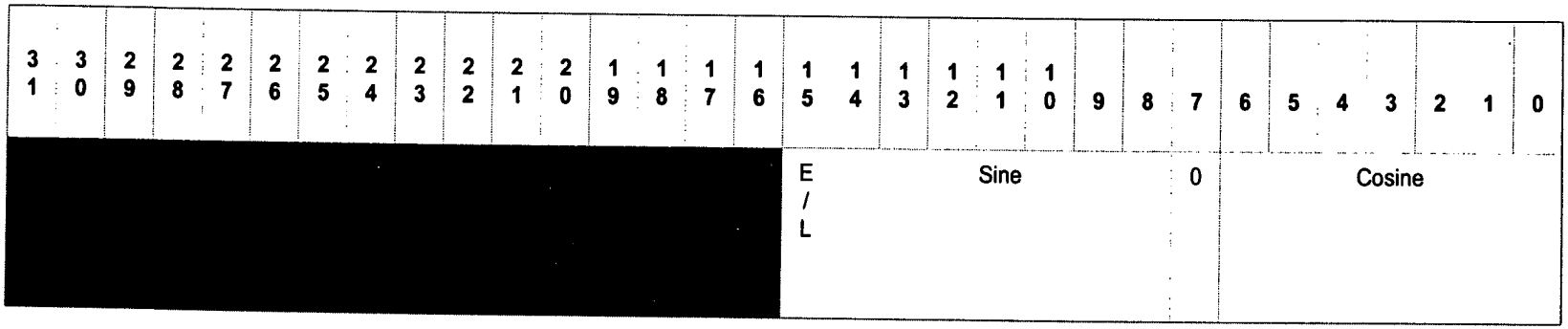

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
E/L
Sine
0
Cosine

FIG. 35

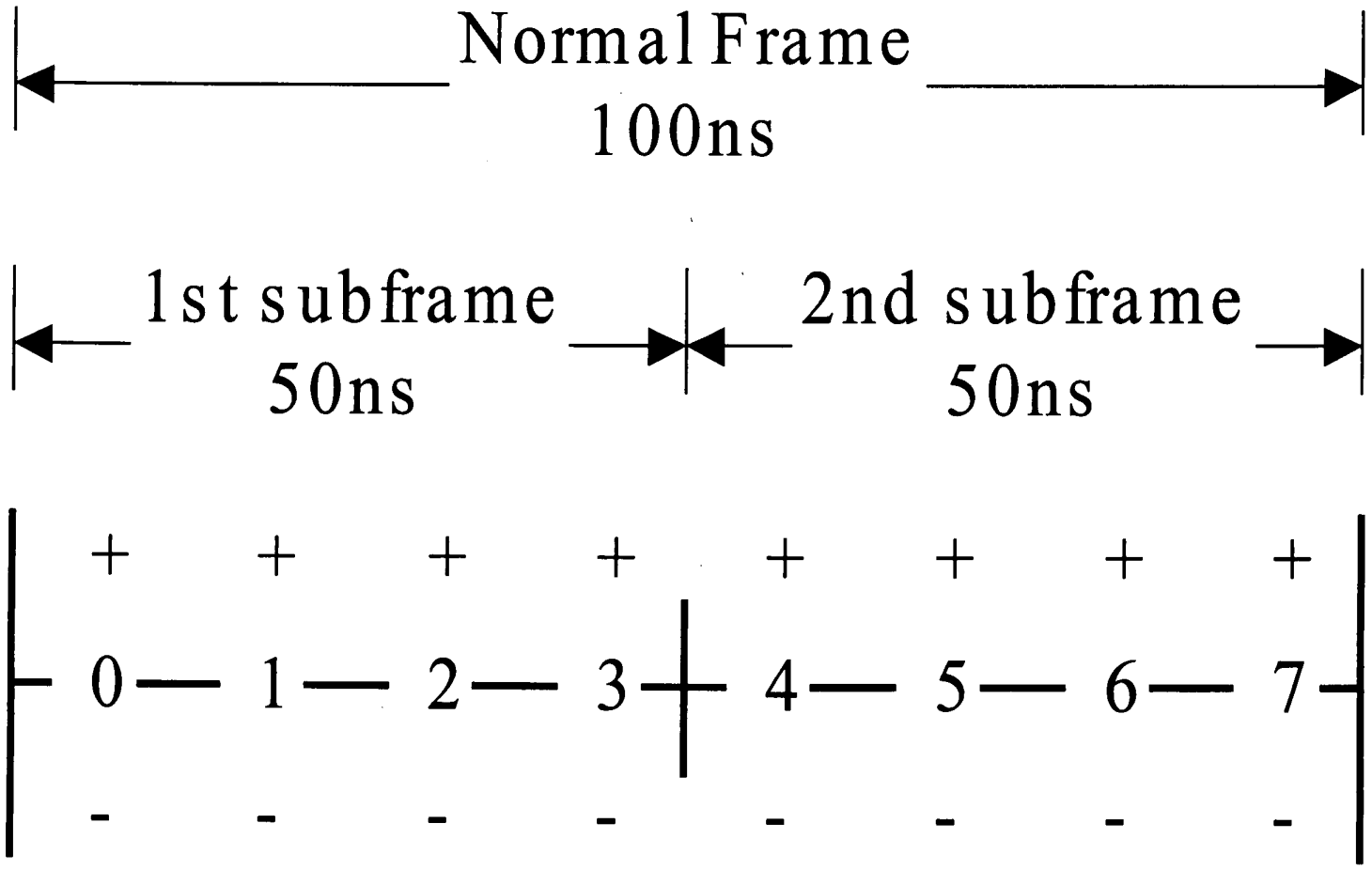

Normal Frame
100ns
1st subframe
50ns
2nd subframe
50ns
+ + + + + + + +
0 1 2 3 4 5 6 7
- - - - - - - -

FIG. 36

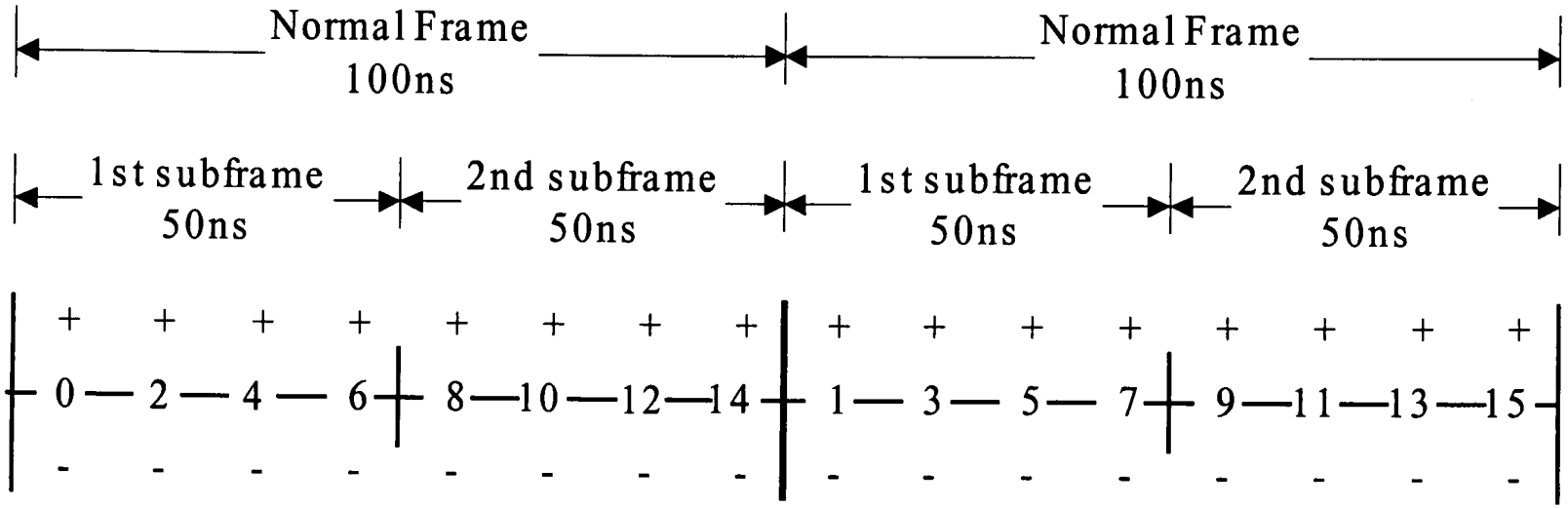

Normal Frame
100ns
Normal Frame
100ns
1st subframe
50ns
2nd subframe
50ns
1st subframe
50ns
2nd subframe
50ns
+ + + + + + + + + + + + + + + +
0 2 4 6 8 10 12 14 1 3 5 7 9 11 13 15
- - - - - - - - - - - - - - - -

FIG. 37

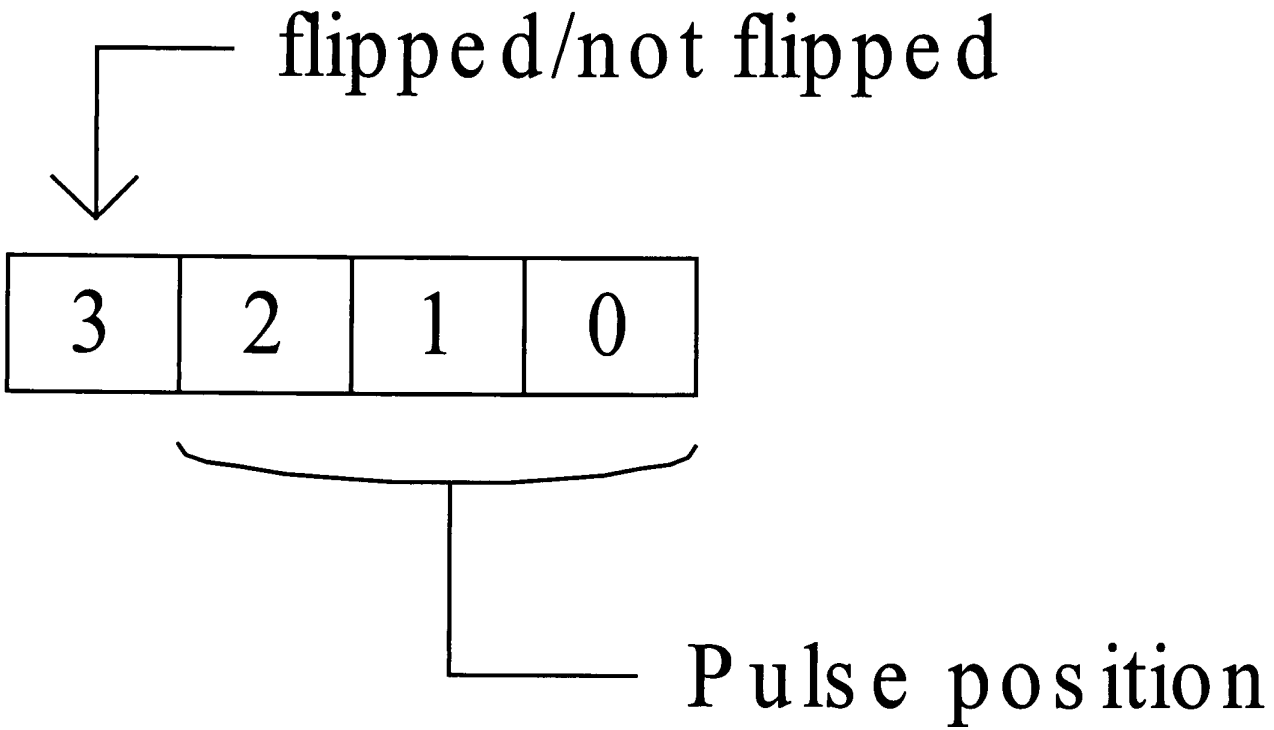


FIG. 38

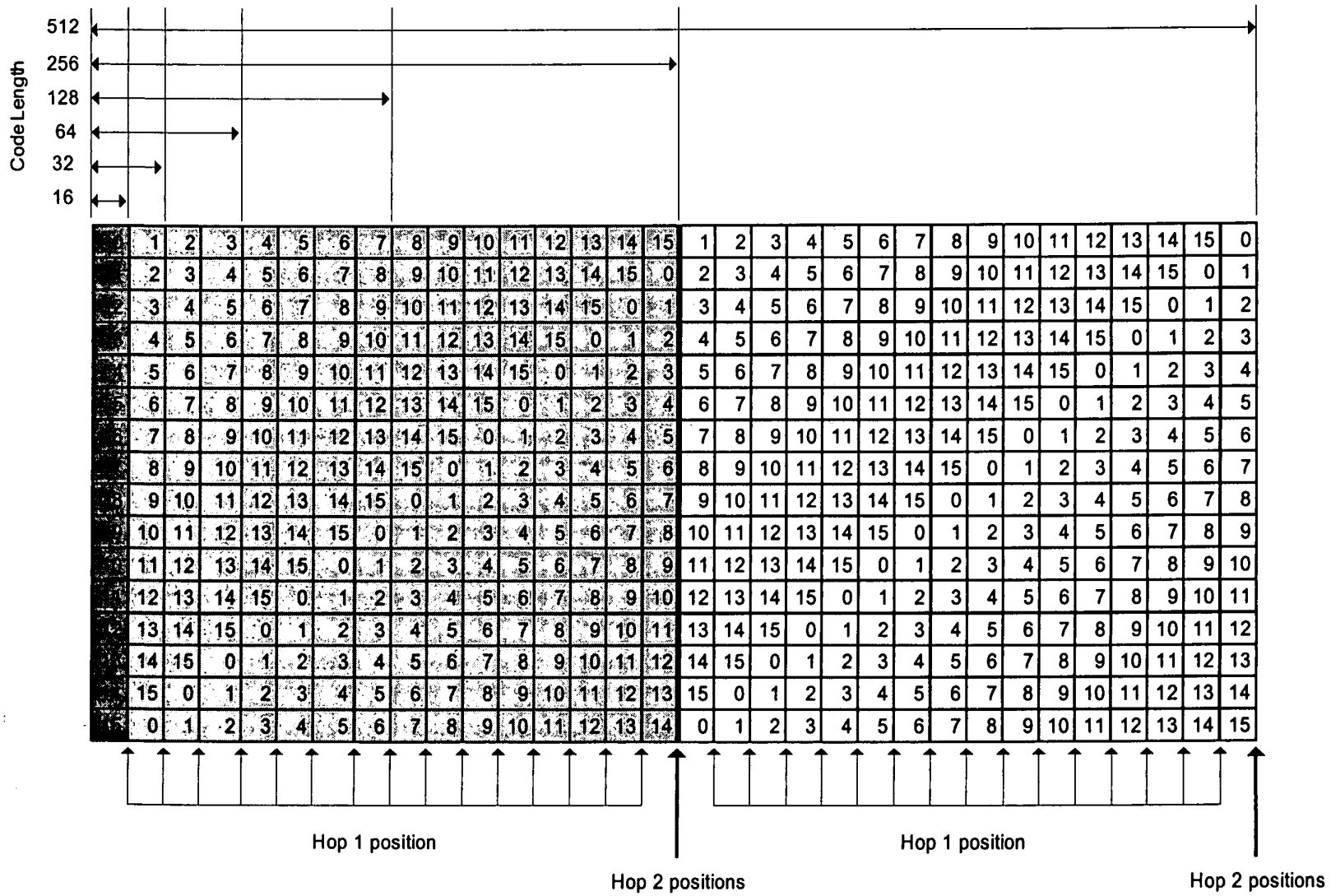

Code Length
512
256
128
64
32
16
Hop 1 position
Hop 2 positions
Hop 1 position
Hop 2 positions

FIG. 39

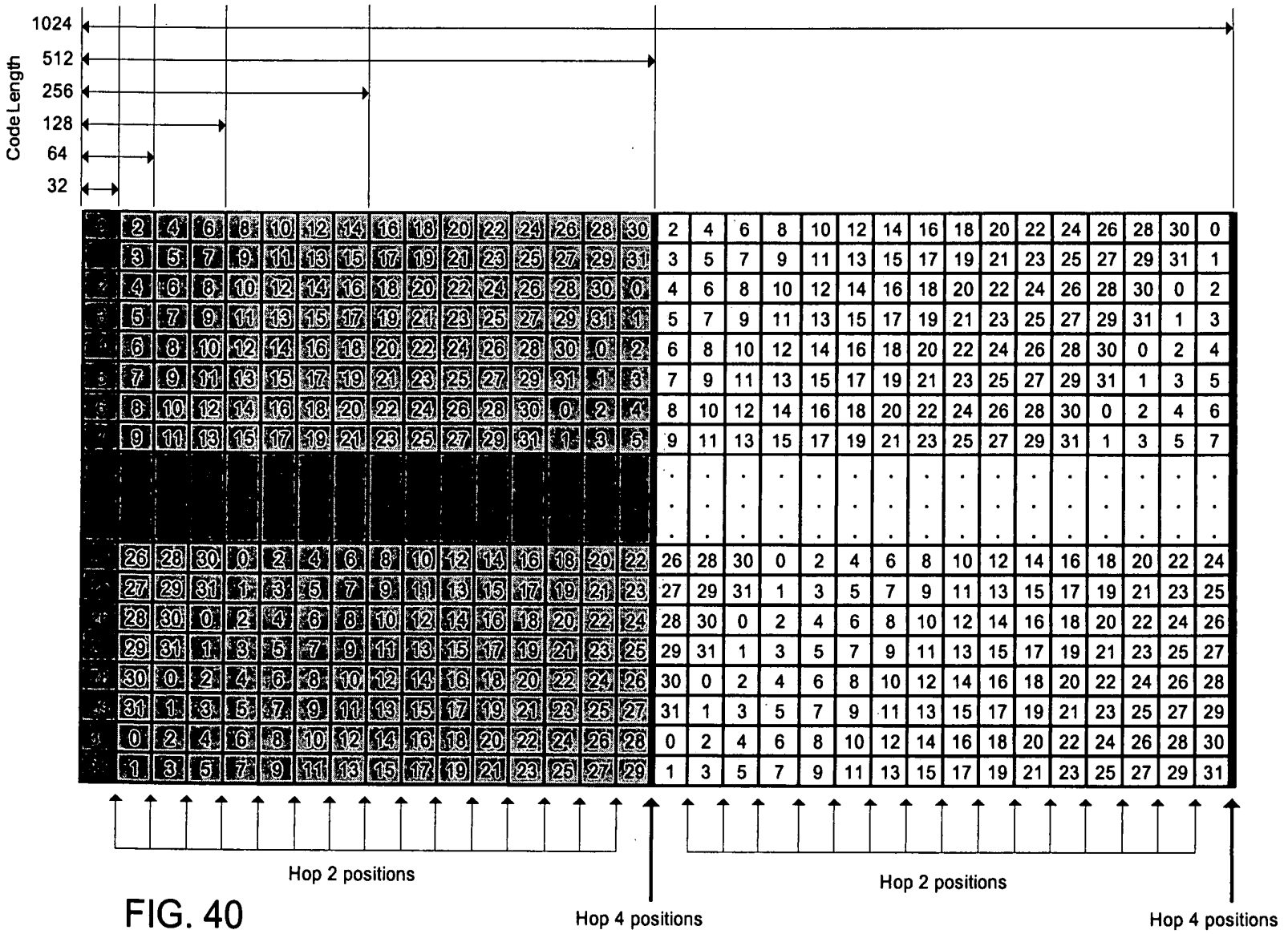

Code Length
1024
512
256
128
64
32
Hop 2 positions
Hop 4 positions
Hop 2 positions
Hop 4 positions

FIG. 40

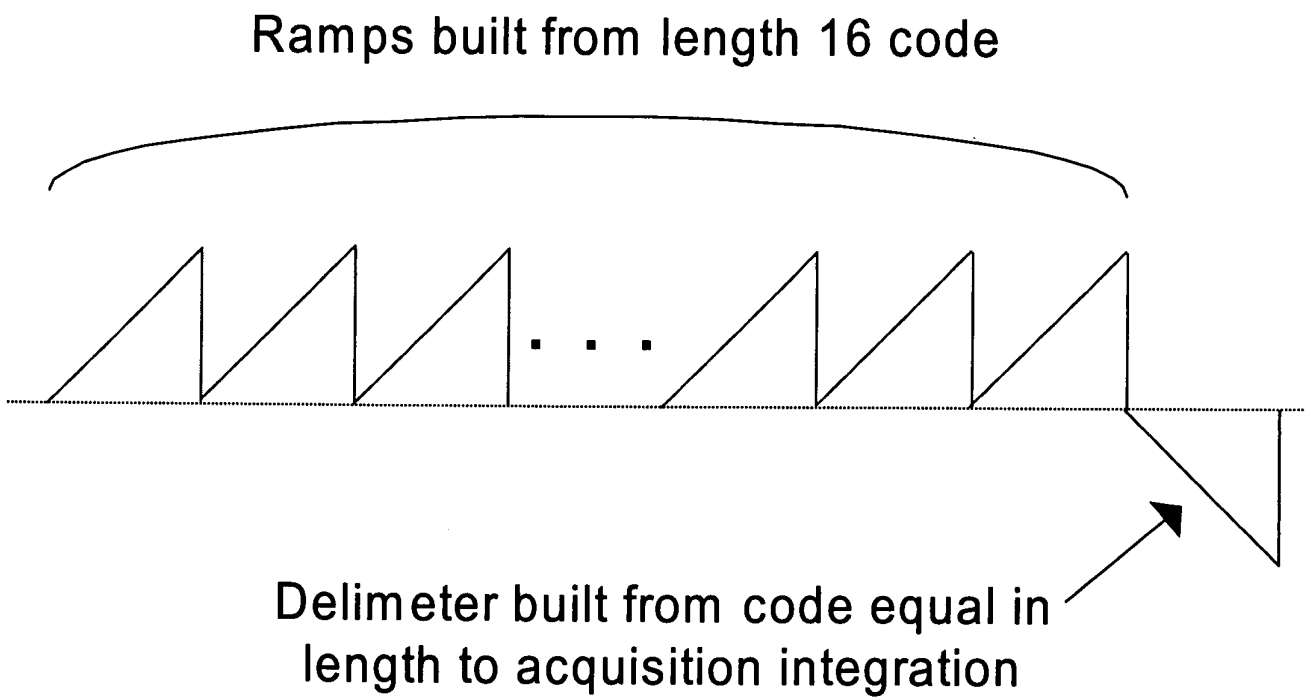

Ramps built from length 16 code
Delimeter built from code equal in length to acquisition integration

FIG. 41

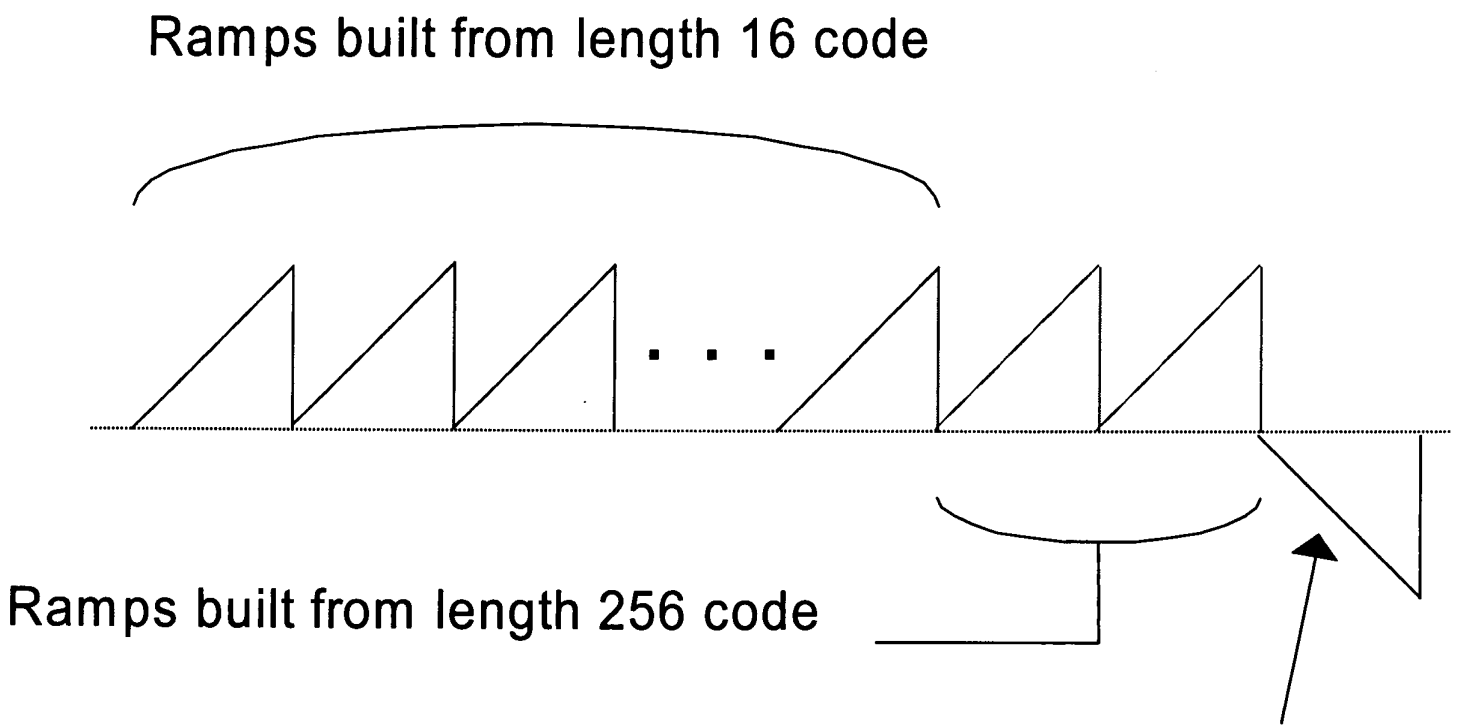

Ramps built from length 16 code
Ramps built from length 256 code
Delimeter built from code equal in length to acquisition integration

FIG. 42

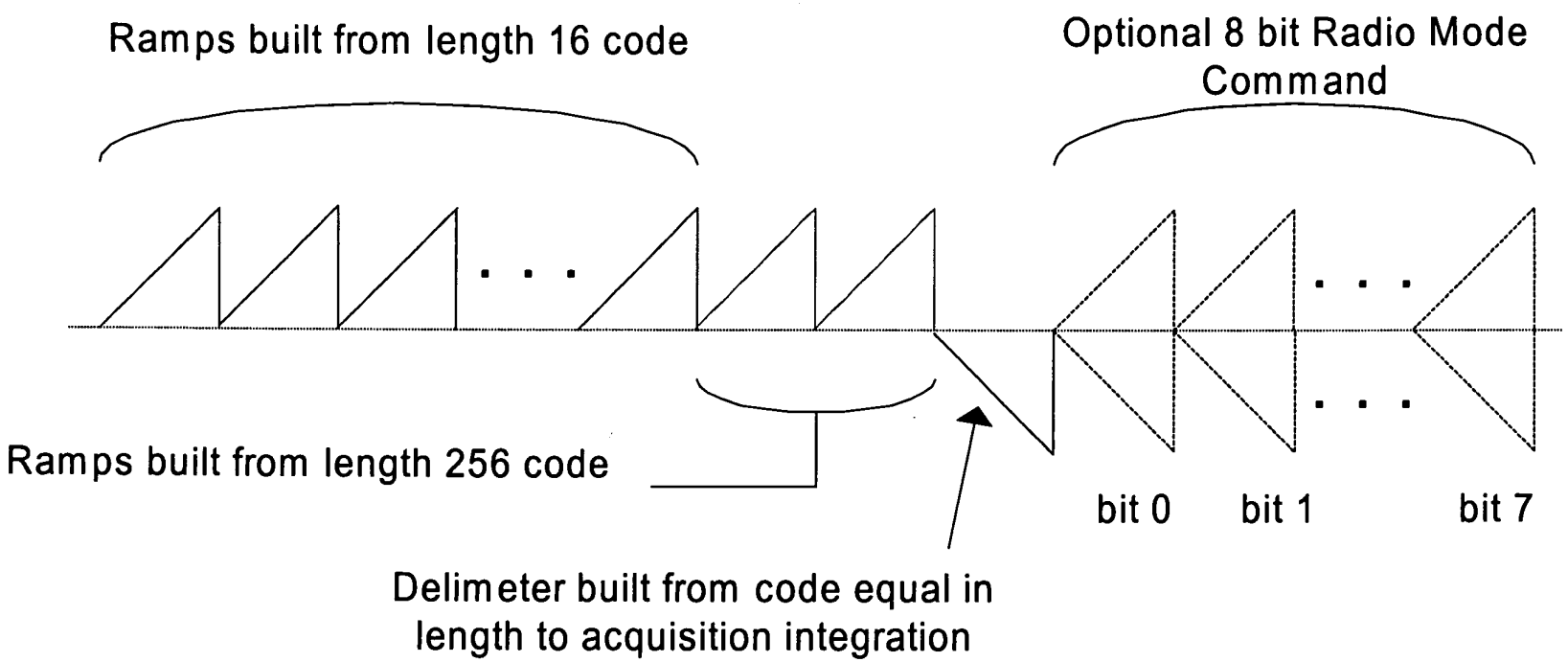

Ramps built from length 16 code
Optional 8 bit Radio Mode Command
Ramps built from length 256 code
bit 0
bit 1
bit 7
Delimeter built from code equal in length to acquisition integration

FIG. 43

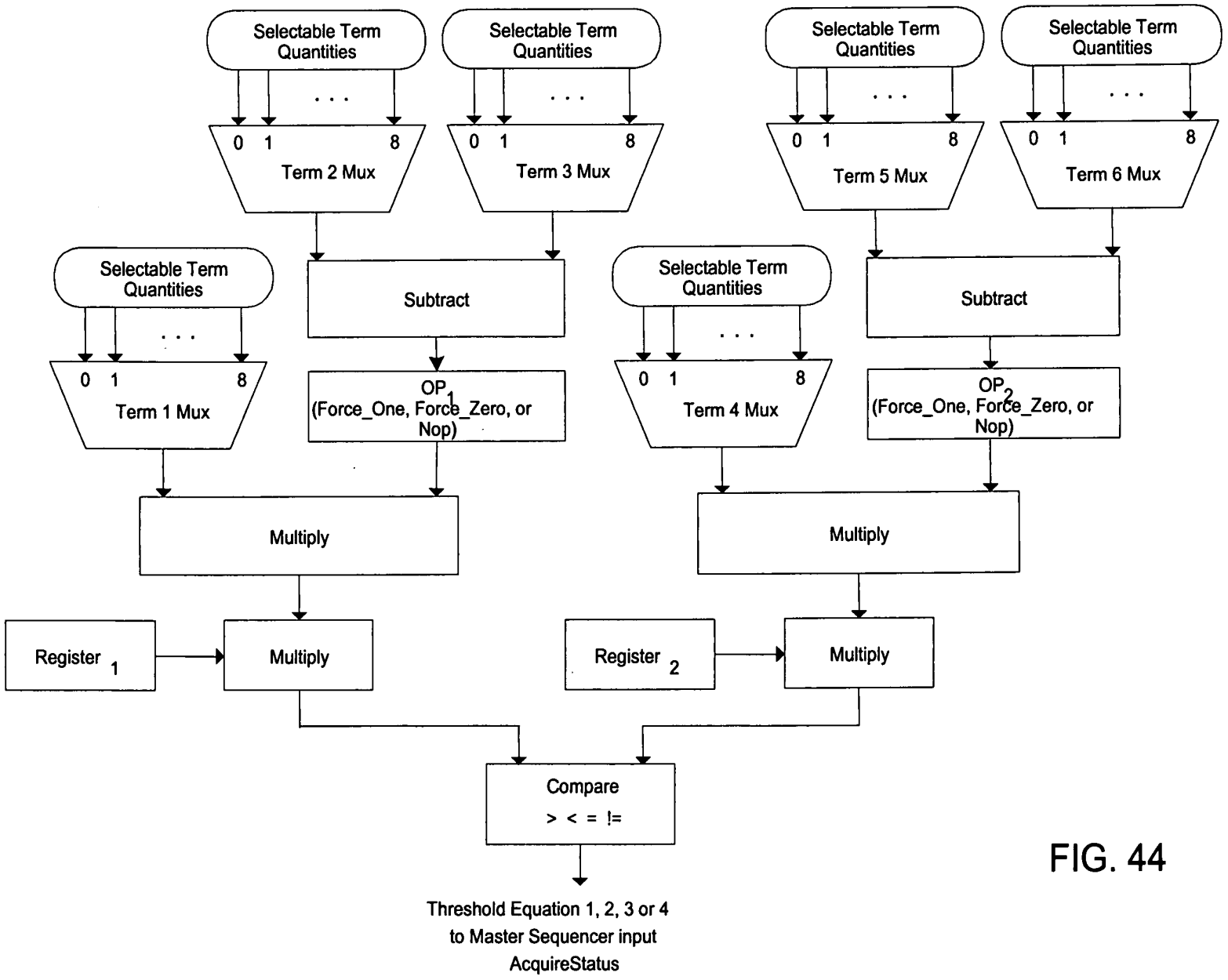

Selectable Term Quantities
Selectable Term Quantities
Selectable Term Quantities
Selectable Term Quantities
0 1 8
Term 2 Mux
0 1 8
Term 3 Mux
0 1 8
Term 5 Mux
0 1 8
Term 6 Mux
Selectable Term Quantities
Subtract
Selectable Term Quantities
Subtract
0 1 8
Term 1 Mux
OP1 (Force_One, Force_Zero, or Nop)
0 1 8
Term 4 Mux
OP2 (Force_One, Force_Zero, or Nop)
Multiply
Multiply
Register 1
Multiply
Register 2
Multiply
Compare
> < = !=
Threshold Equation 1, 2, 3 or 4 to Master Sequencer input AcquireStatus

FIG. 44

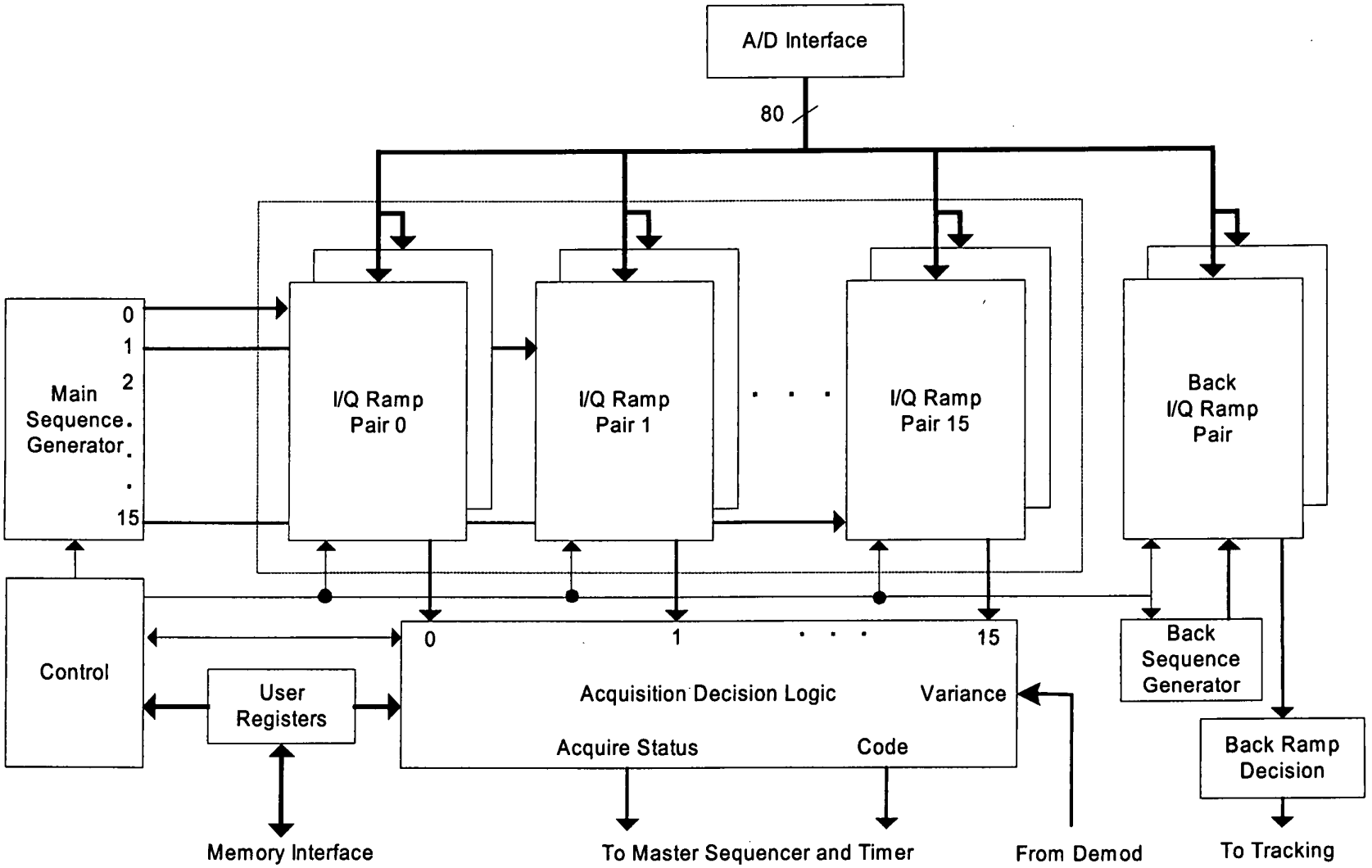

A/D Interface
80
Main Sequence Generator
0
1
2
15
I/Q Ramp Pair 0
I/Q Ramp Pair 1
I/Q Ramp Pair 15
Back I/Q Ramp Pair
Control
User Registers
0
1
15
Acquisition Decision Logic
Variance
Acquire Status
Code
Back Sequence Generator
Back Ramp Decision
Memory Interface
To Master Sequencer and Timer
From Demod
To Tracking

FIG. 45

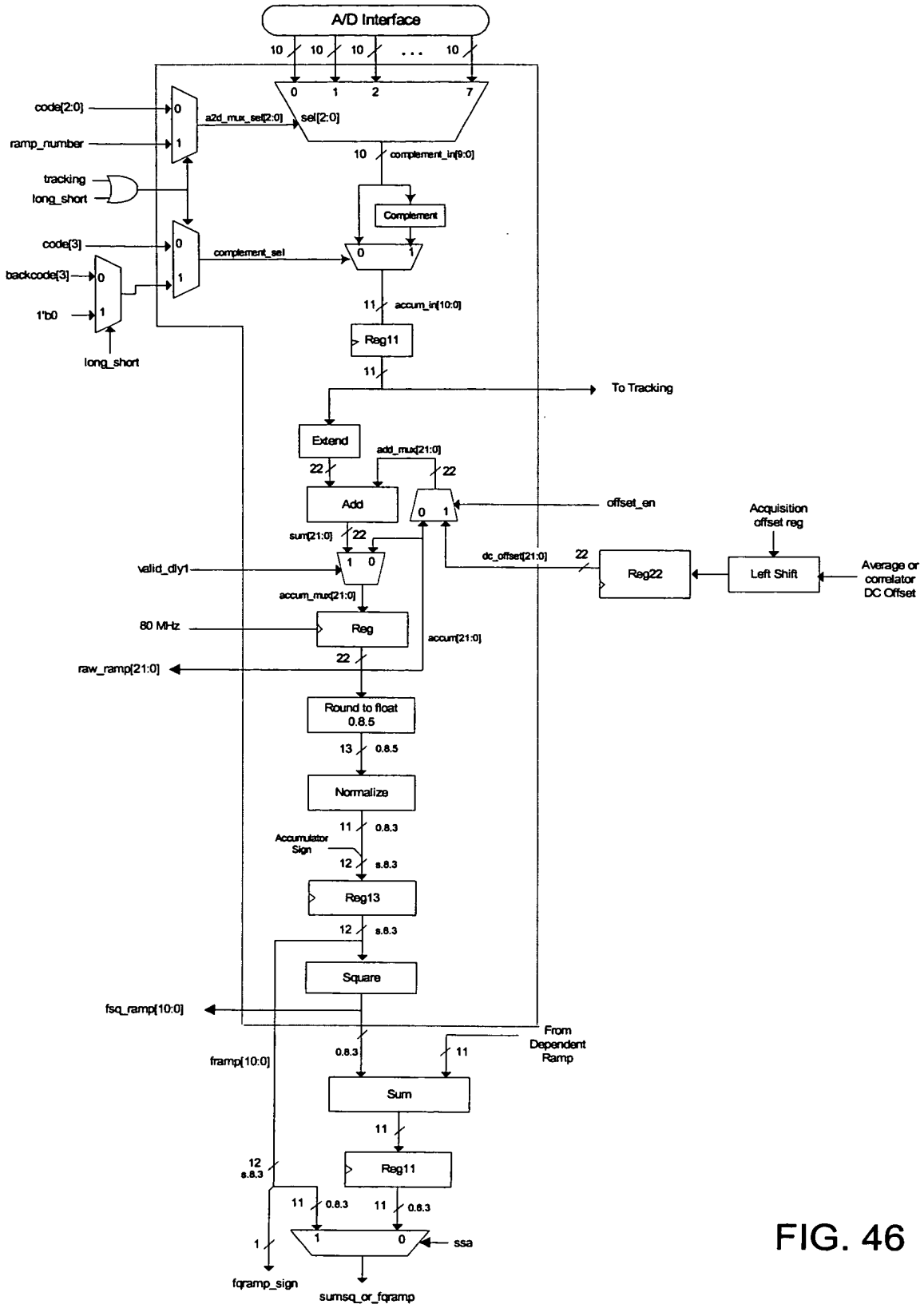
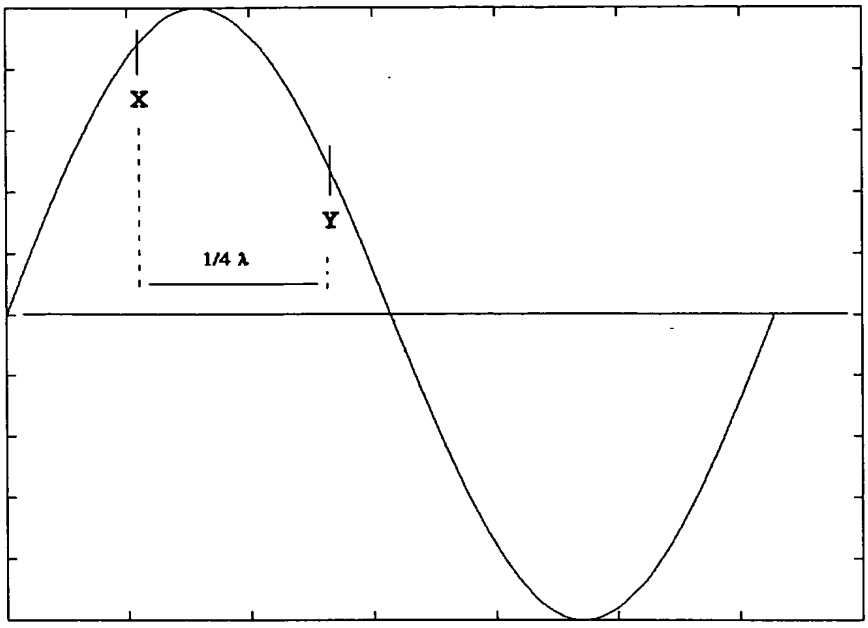

A/D Interface
10
10
10
...
10
0
1
2
7
code[2:0]
ramp_number
a2d_mux_sel[2:0]
sel[2:0]
10
complement_in[9:0]
tracking
long_short
Complement
code[3]
backcode[3]
1'b0
long_short
complement_sel
11
accum_in[10:0]
Reg11
11
To Tracking
Extend
add_mux[21:0]
22
22
Add
offset_en
Acquisition offset reg
sum[21:0]
22
valid_dly1
dc_offset[21:0]
22
Reg22
Left Shift
Average or correlator DC Offset
accum_mux[21:0]
80 MHz
Reg
accum[21:0]
22
raw_ramp[21:0]
Round to float 0.8.5
13
0.8.5
Normalize
11
0.8.3
Accumulator Sign
12
s.8.3
Reg13
12
s.8.3
Square
fsq_ramp[10:0]
From Dependent Ramp
framp[10:0]
0.8.3
11
Sum
11
12
s.8.3
Reg11
11
0.8.3
11
0.8.3
1
ssa
fqramp_sign
sumsq_or_fqramp

FIG. 46



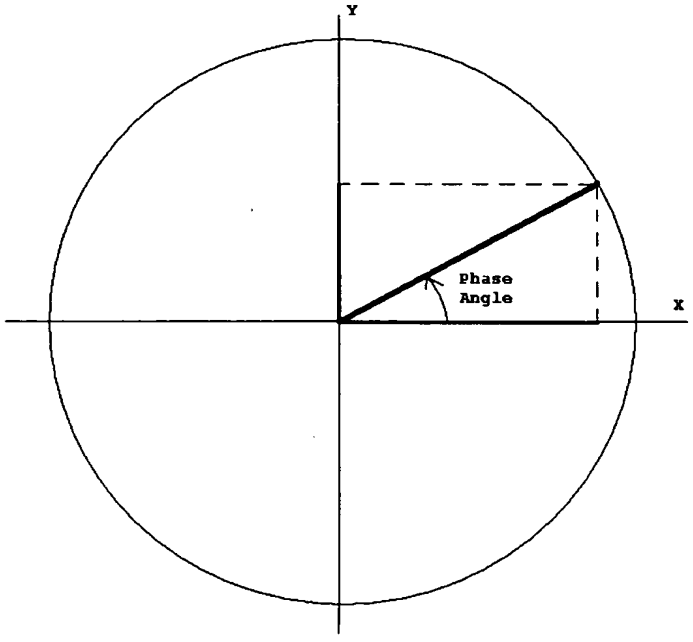


FIG. 47

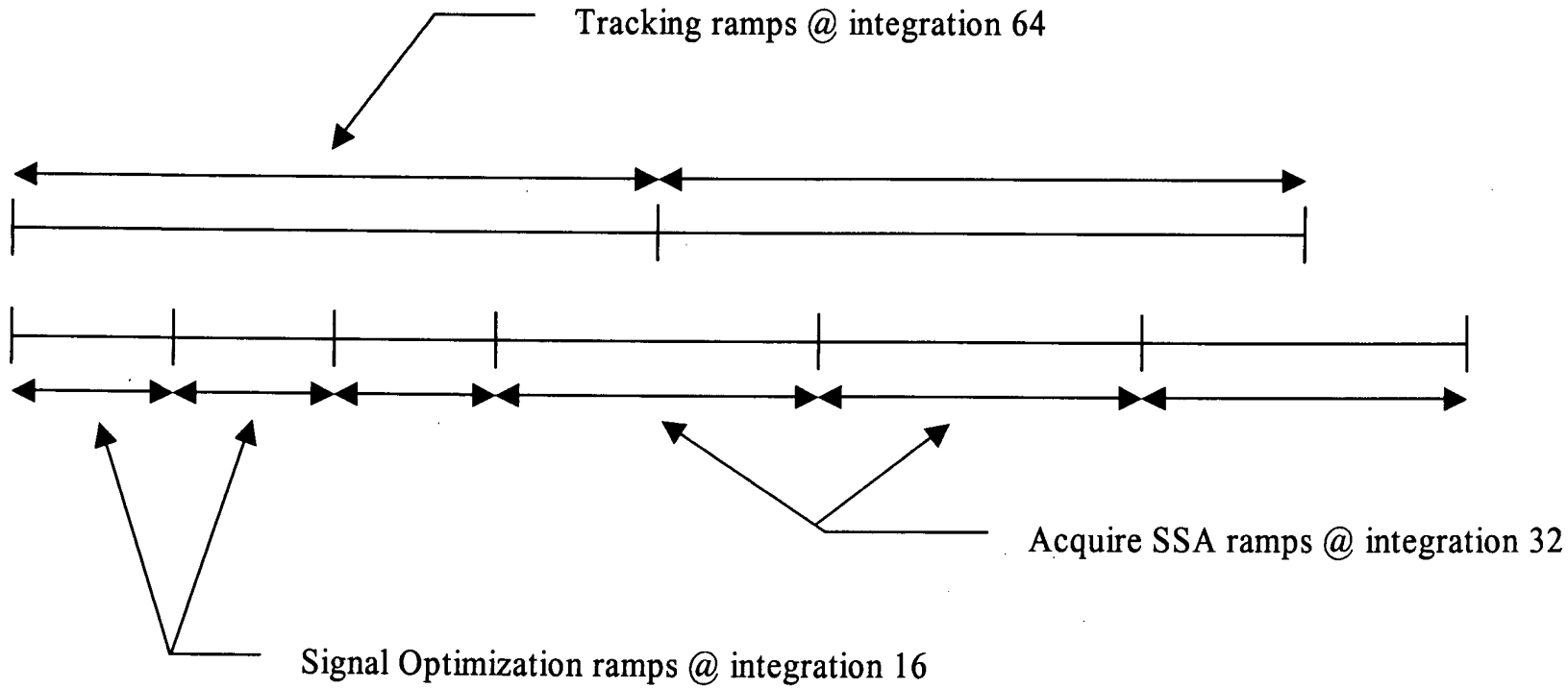

Tracking ramps @ integration 64
Acquire SSA ramps @ integration 32
Signal Optimization ramps @ integration 16

FIG. 48

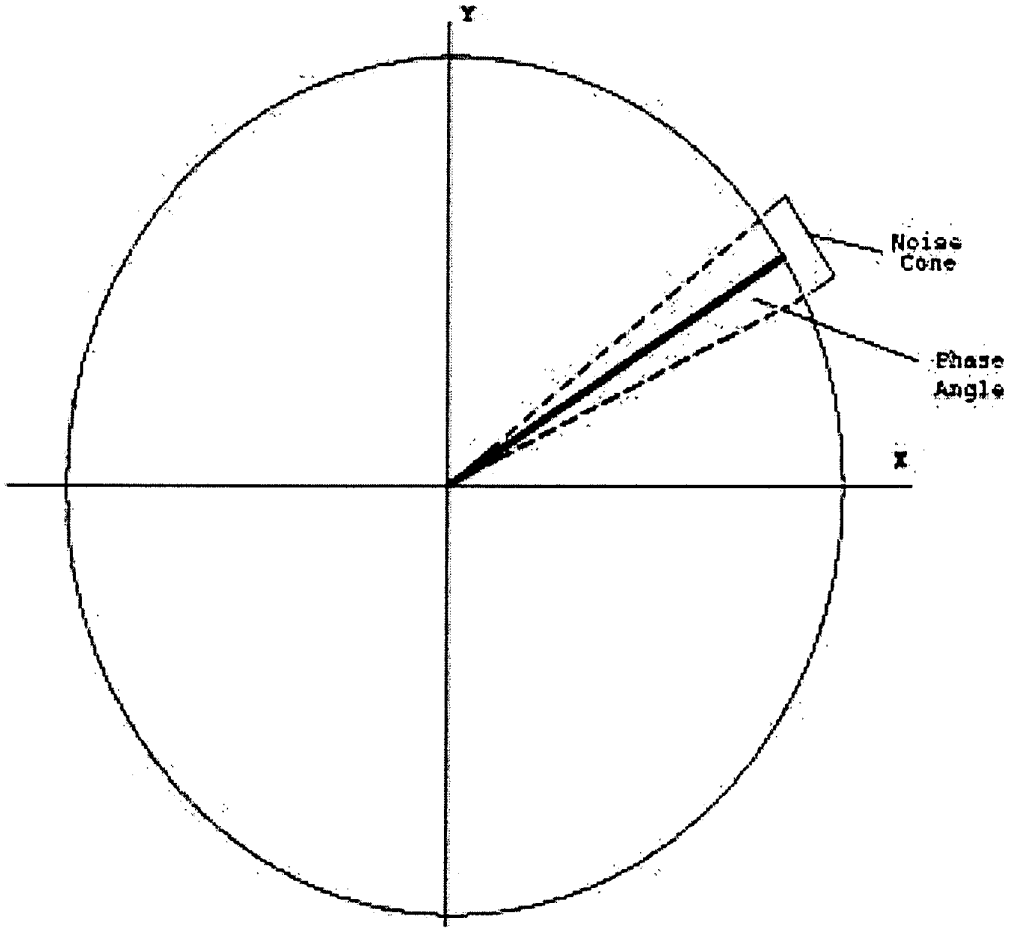


FIG. 49

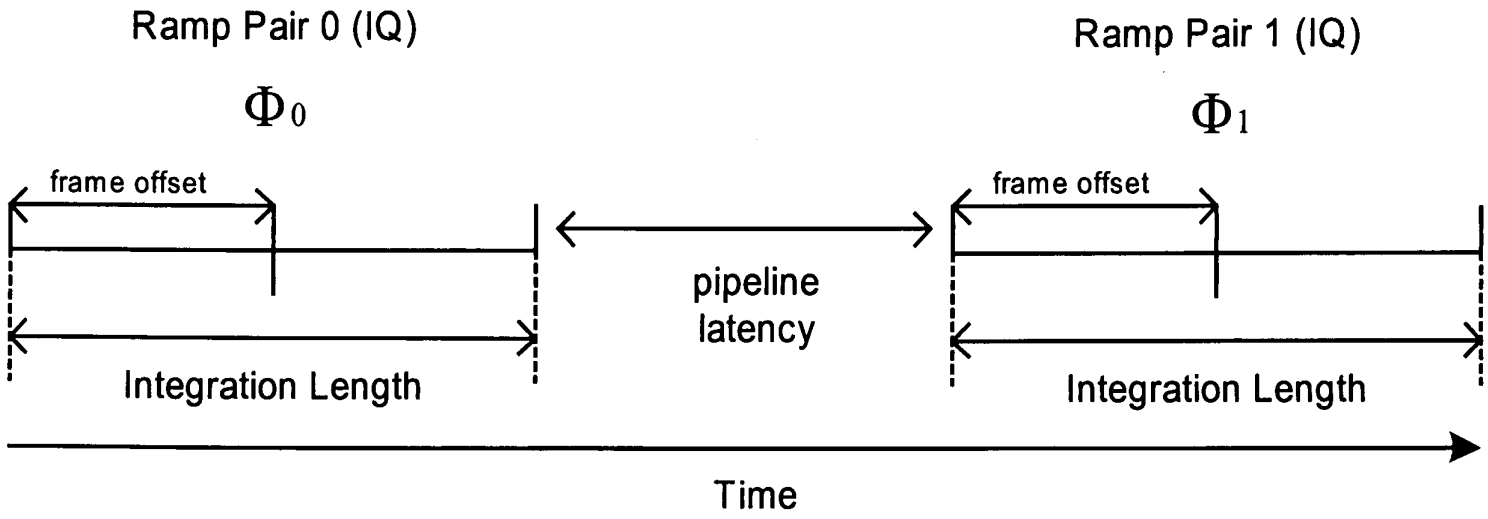

Ramp Pair 0 (IQ)
Φ_0
frame offset
Integration Length
pipeline
latency
Ramp Pair 1 (IQ)
Φ_1
frame offset
Integration Length
Time

FIG. 50

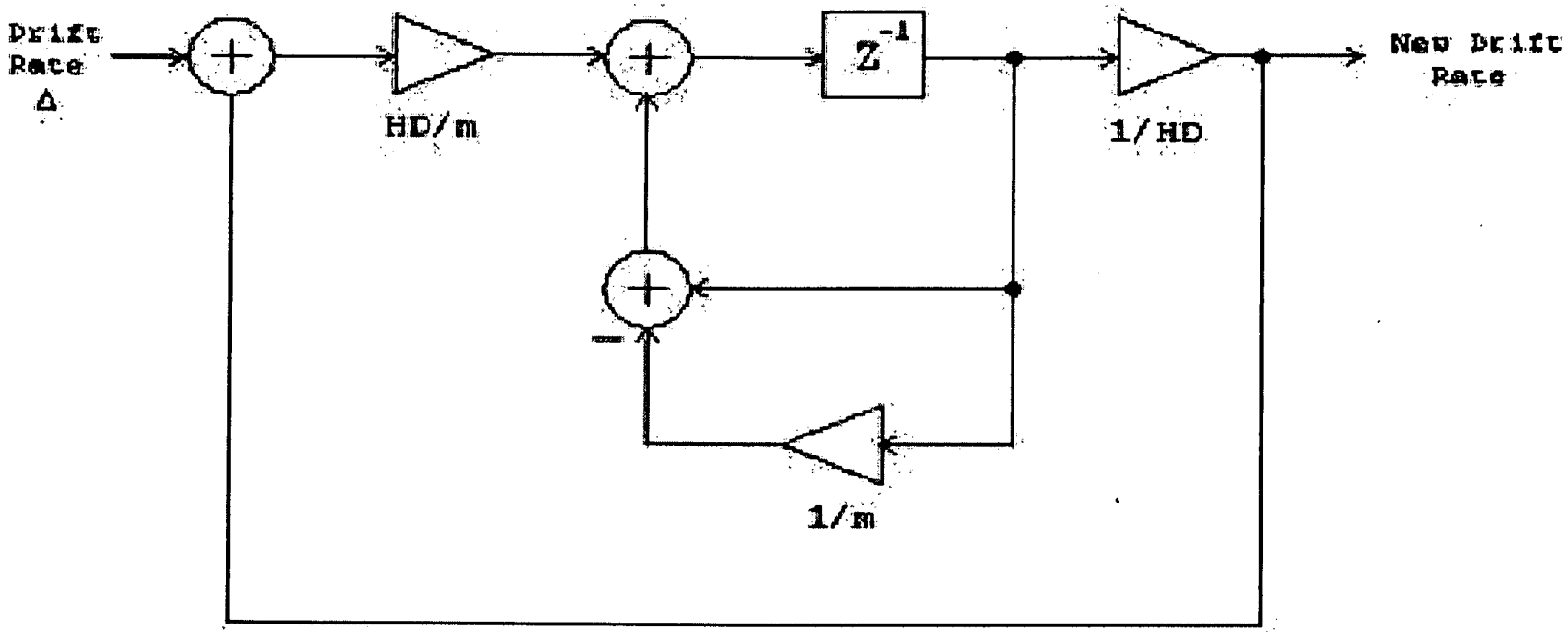


FIG. 51

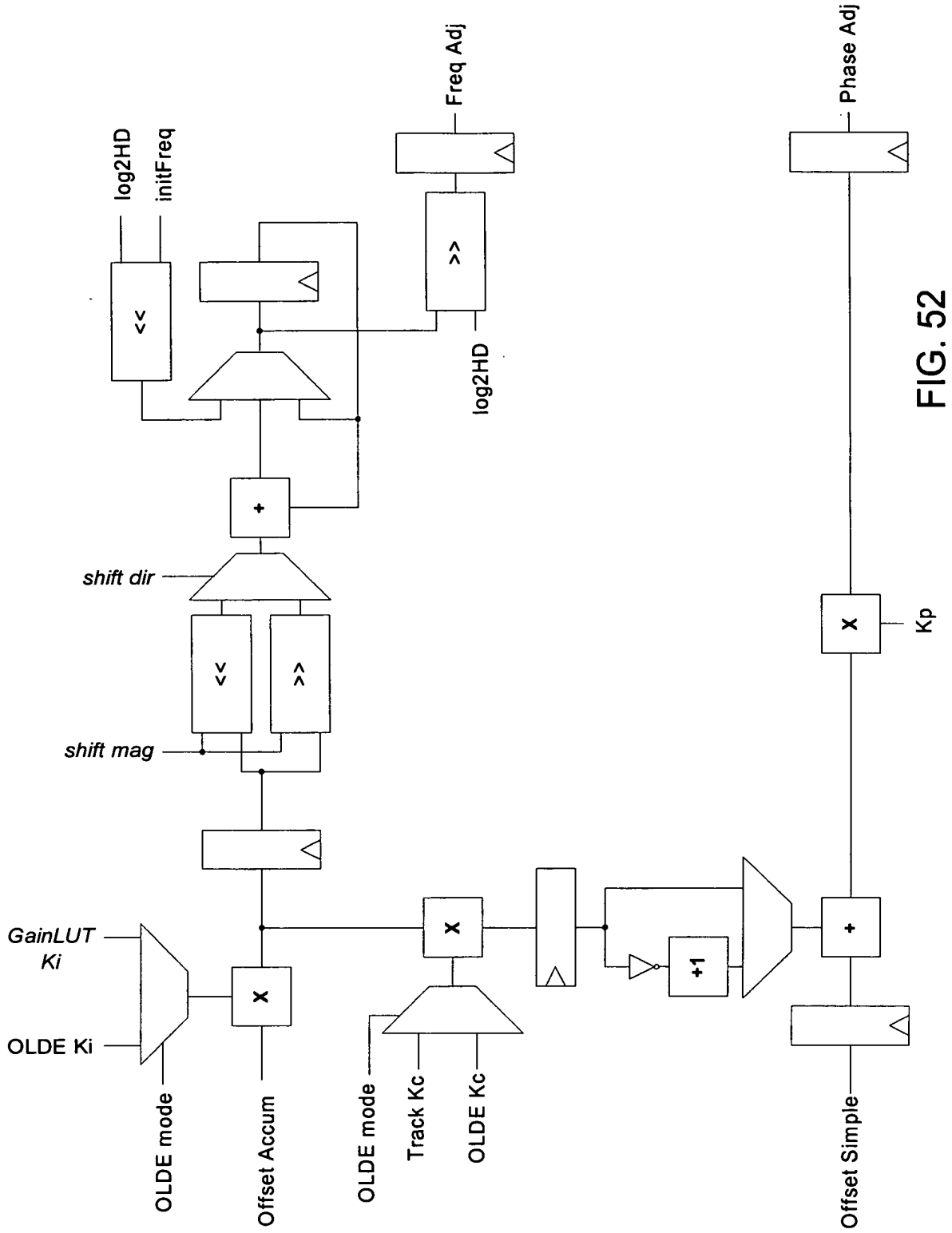

log2HD
initFreq
Freq Adj
Phase Adj
<<
>>
log2HD
+
shift dir
<<
>>
shift mag
GainLUT
Ki
OLDE Ki
X
X
+1
+
X
Kp
OLDE mode
Offset Accum
OLDE mode
Track Kc
OLDE Kc
Offset Simple

FIG. 52

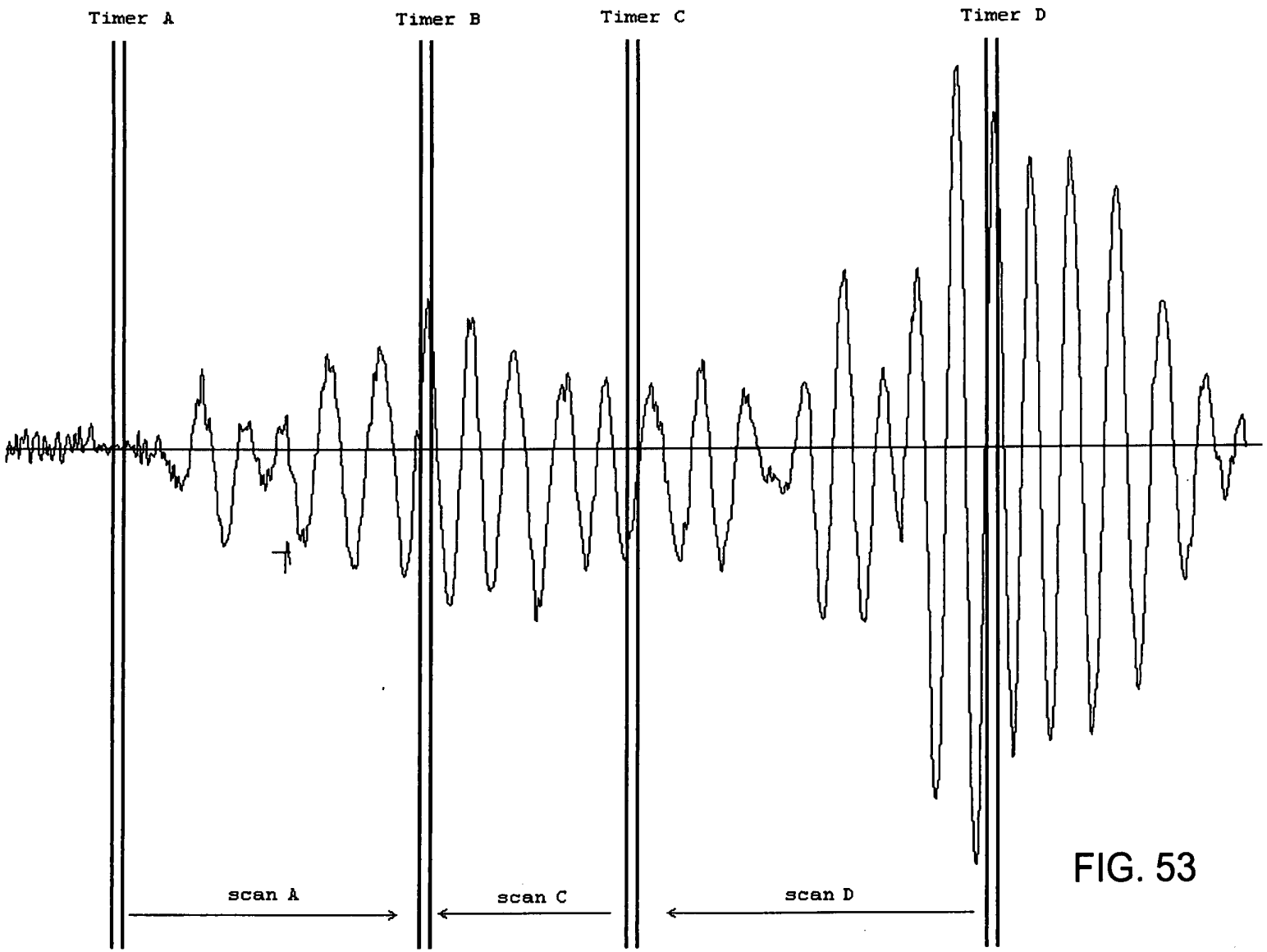


FIG. 53

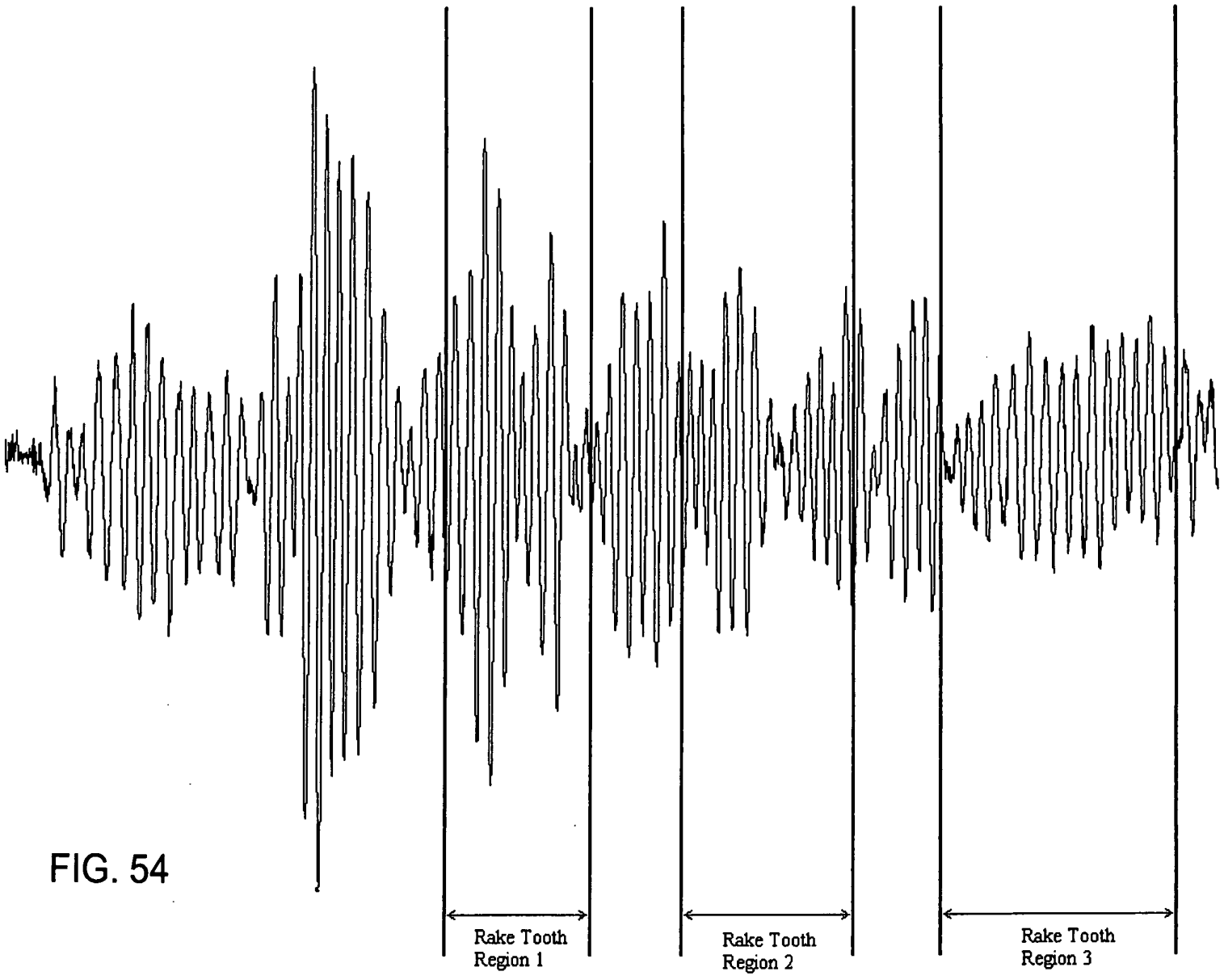


FIG. 54

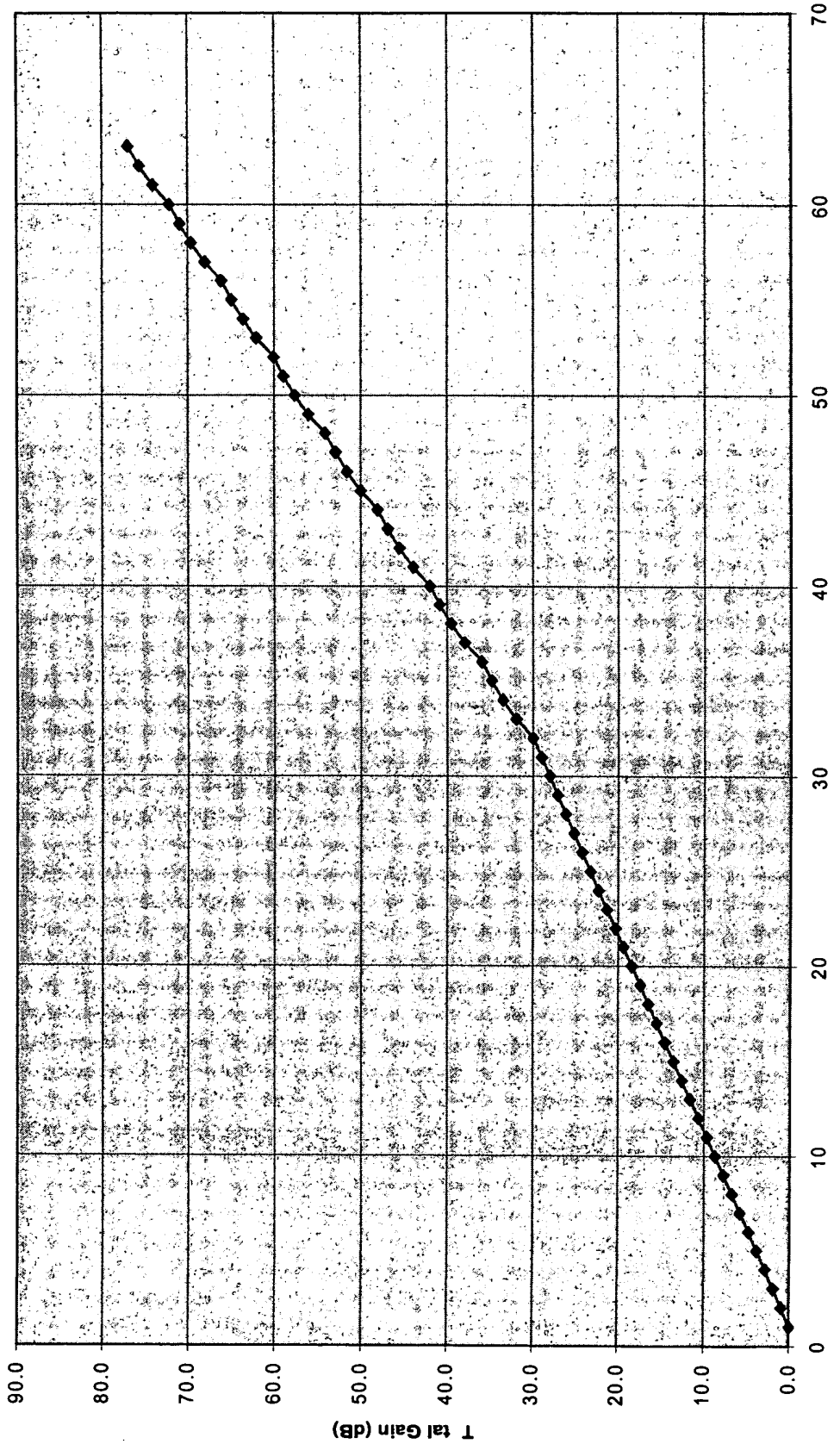

90.0
80.0
70.0
60.0
50.0
40.0
30.0
20.0
10.0
0.0
T tal Gain (dB)
0
10
20
30
40
50
60
70
Digital Control Value

FIG. 55

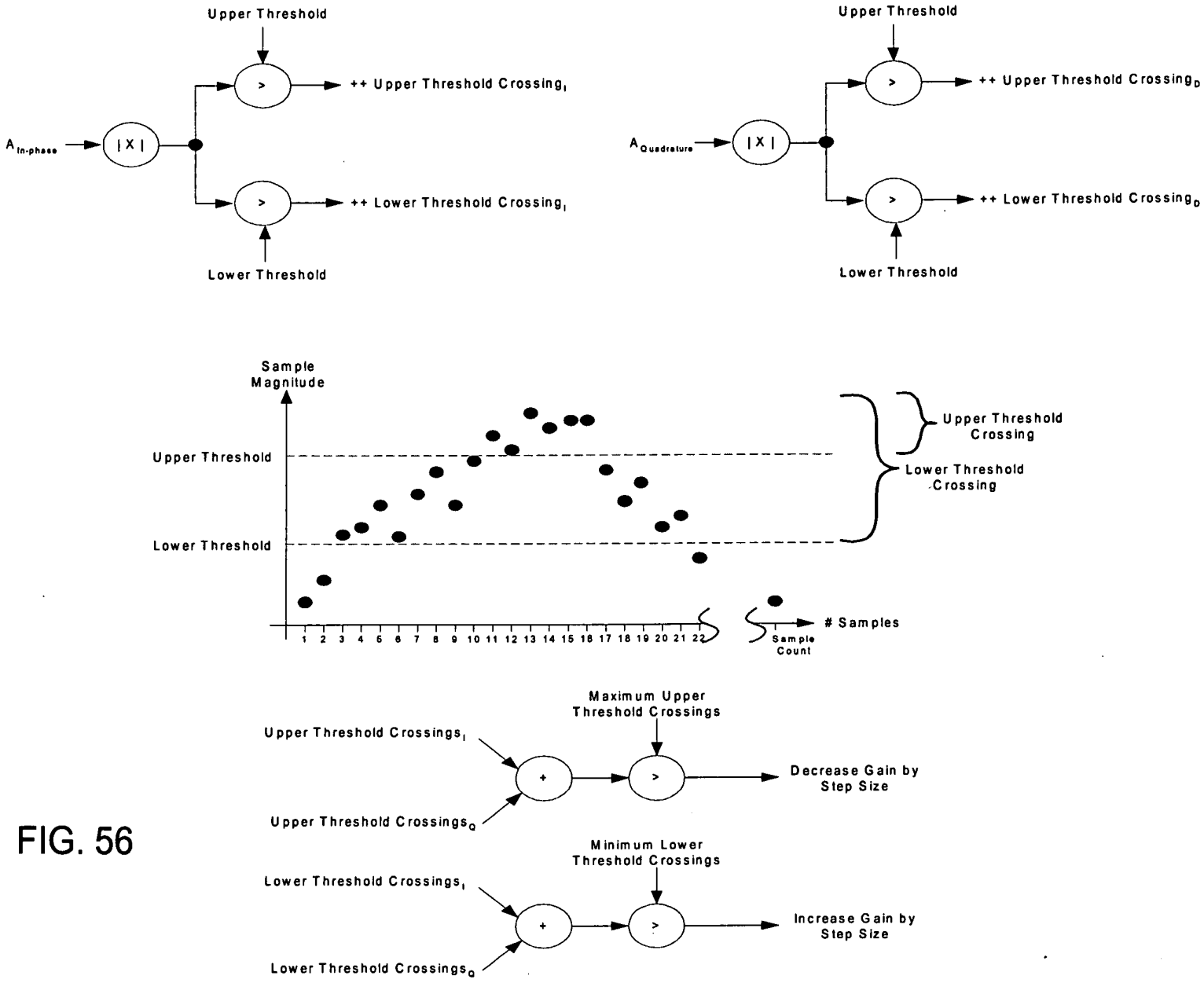

Upper Threshold
A In-phase
| X |
++ Upper Threshold Crossing I
++ Lower Threshold Crossing I
Lower Threshold
Upper Threshold
A Quadrature
| X |
++ Upper Threshold Crossing Q
++ Lower Threshold Crossing Q
Lower Threshold
Sample Magnitude
Upper Threshold
Lower Threshold
Upper Threshold Crossing
Lower Threshold Crossing
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22
Sample Count
Samples
Maximum Upper Threshold Crossings
Upper Threshold Crossings I
Upper Threshold Crossings Q
Decrease Gain by Step Size
Minimum Lower Threshold Crossings
Lower Threshold Crossings I
Lower Threshold Crossings Q
Increase Gain by Step Size

FIG. 56

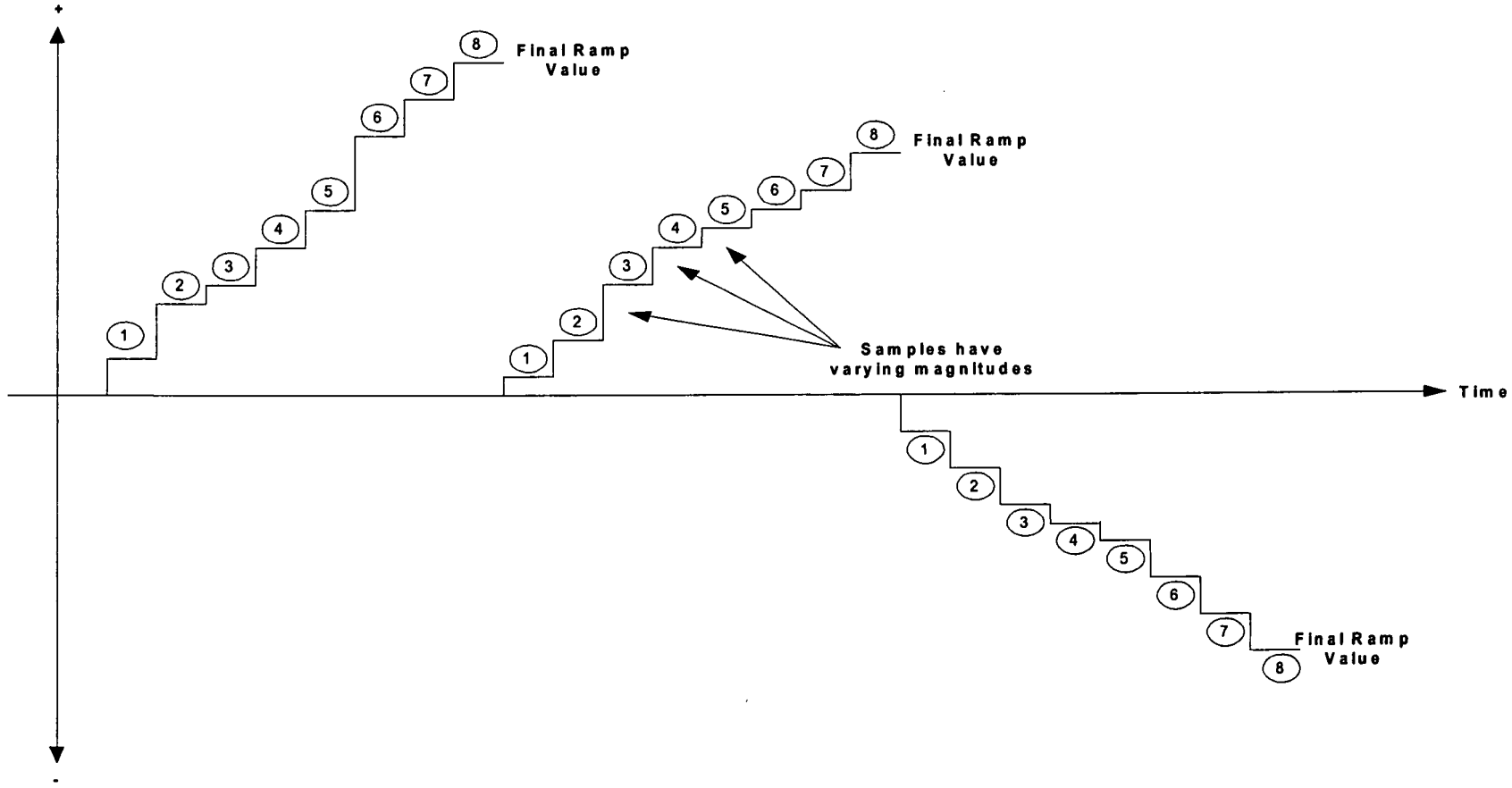

+
-
1
2
3
4
5
6
7
8
Final Ramp Value
Samples have varying magnitudes
Time

FIG. 57

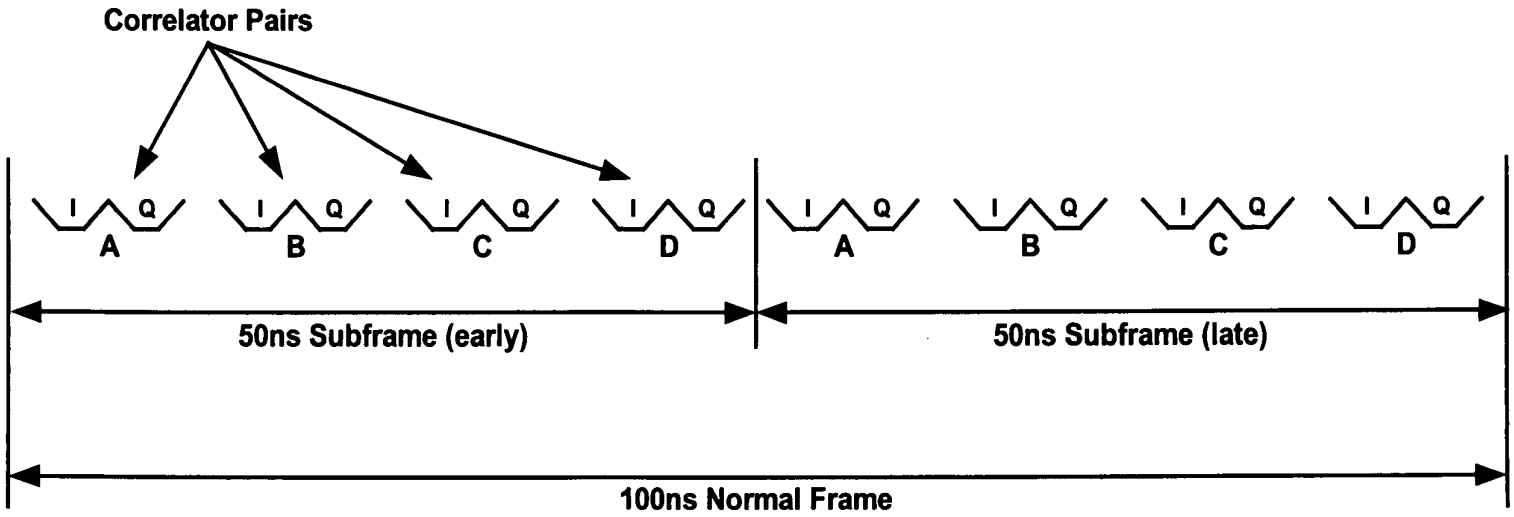

Correlator Pairs
I
Q
A
B
C
D
50ns Subframe (early)
50ns Subframe (late)
100ns Normal Frame

FIG. 58

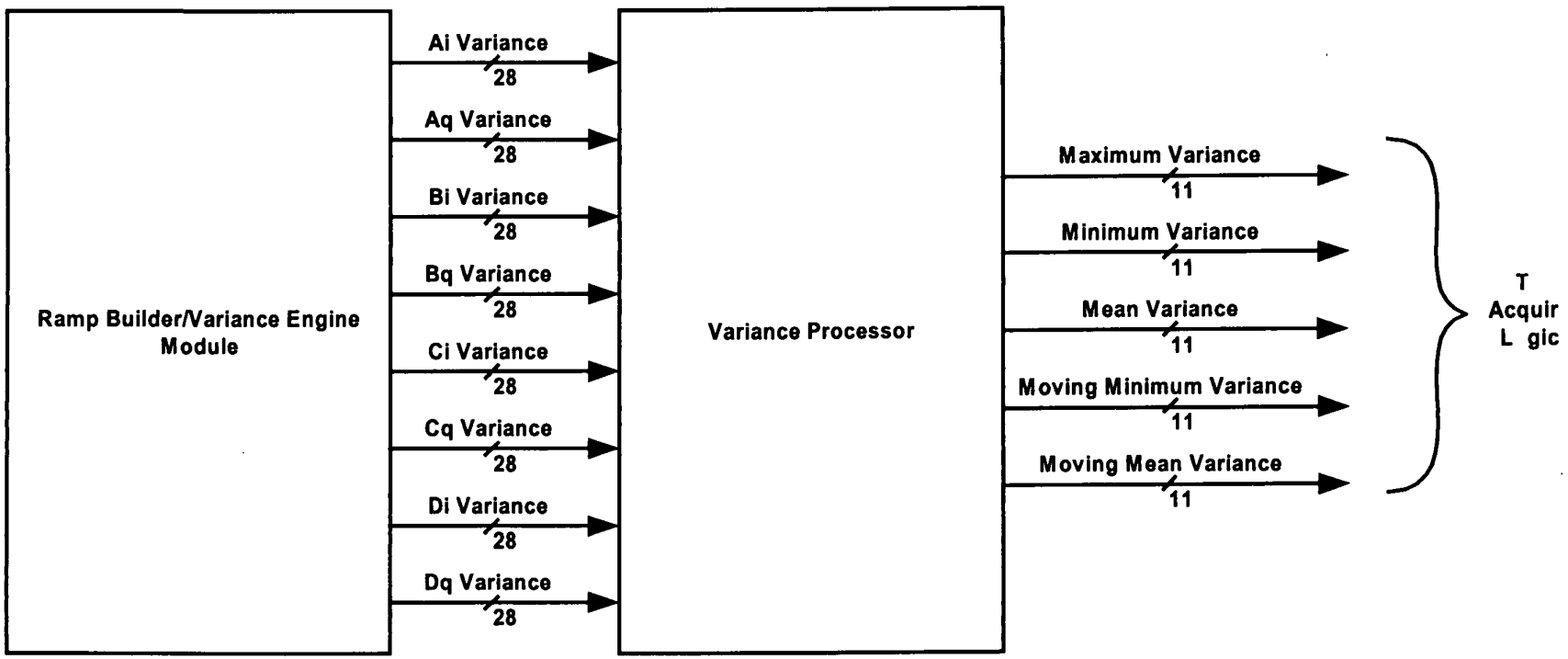

Ramp Builder/Variance Engine Module
Ai Variance
28
Aq Variance
28
Bi Variance
28
Bq Variance
28
Ci Variance
28
Cq Variance
28
Di Variance
28
Dq Variance
28
Variance Processor
Maximum Variance
11
Minimum Variance
11
Mean Variance
11
Moving Minimum Variance
11
Moving Mean Variance
11
T
Acquir
L gic

FIG. 59

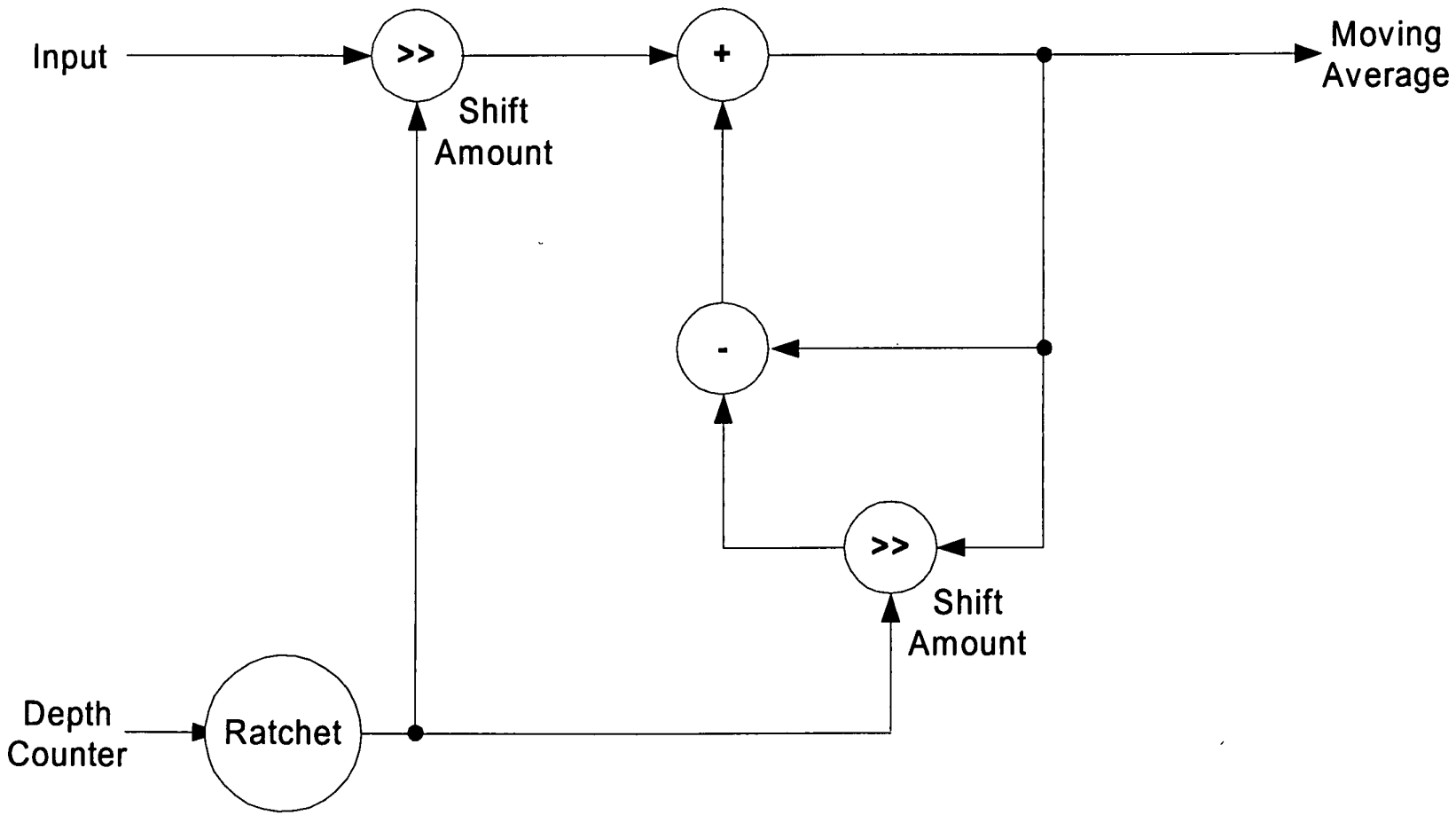

Input
>>
Shift
Amount
+
Moving
Average
-
>>
Shift
Amount
Depth
Counter
Ratchet

FIG. 60

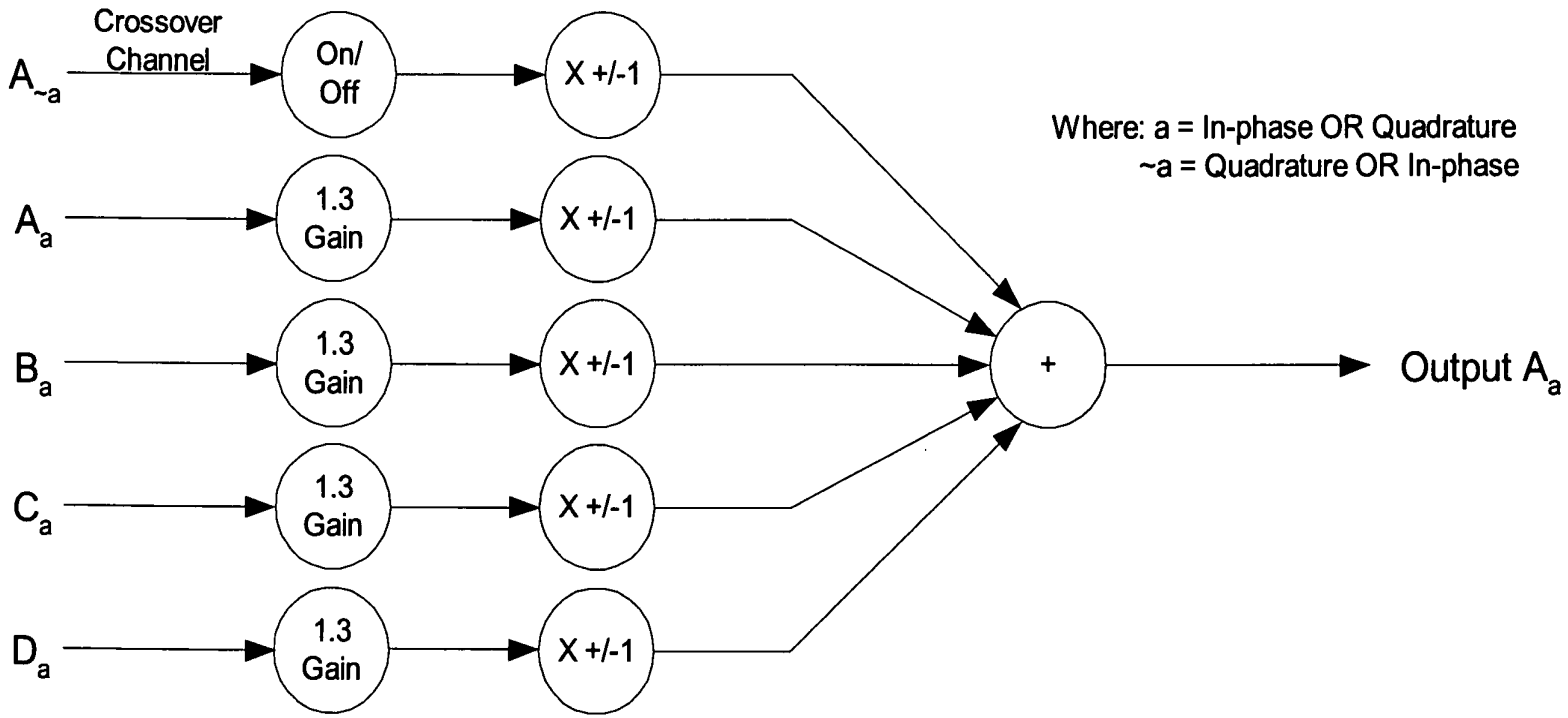
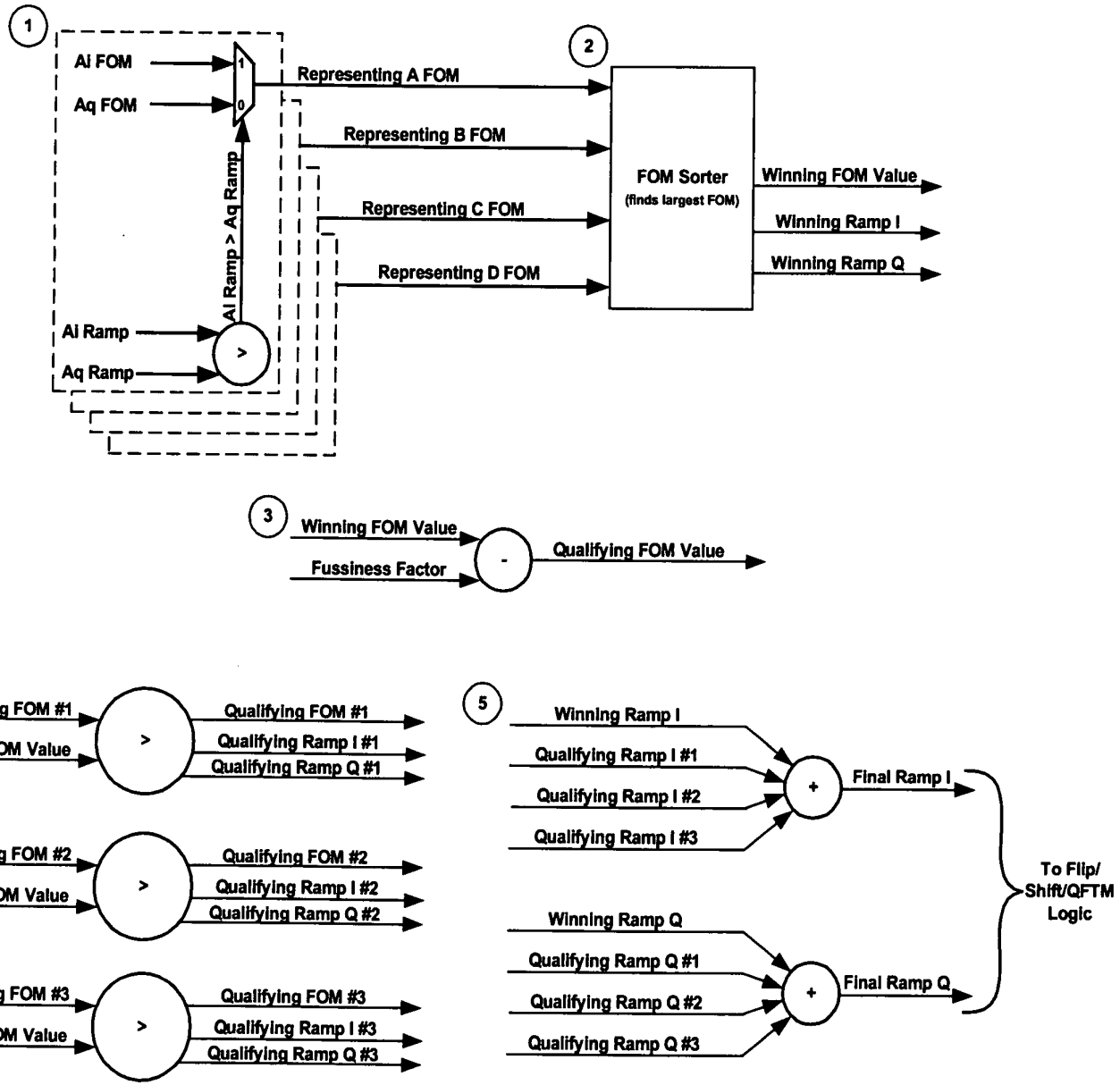

Crossover Channel
$A_{\sim a}$
On/ Off
X +/-1
Where: a = In-phase OR Quadrature
~a = Quadrature OR In-phase
A_a
1.3 Gain
X +/-1
B_a
1.3 Gain
X +/-1
+
Output A_a
C_a
1.3 Gain
X +/-1
D_a
1.3 Gain
X +/-1

FIG. 61

FIG. 62


1
Ai FOM
Aq FOM
1
0
Ai Ramp > Aq Ramp
Ai Ramp
Aq Ramp
>
2
Representing A FOM
Representing B FOM
Representing C FOM
Representing D FOM
FOM Sorter
(finds largest FOM)
Winning FOM Value
Winning Ramp I
Winning Ramp Q
3
Winning FOM Value
Fussiness Factor
-
Qualifying FOM Value
4
non-Winning FOM #1
Qualifying FOM Value
>
Qualifying FOM #1
Qualifying Ramp I #1
Qualifying Ramp Q #1
non-Winning FOM #2
Qualifying FOM Value
>
Qualifying FOM #2
Qualifying Ramp I #2
Qualifying Ramp Q #2
non-Winning FOM #3
Qualifying FOM Value
>
Qualifying FOM #3
Qualifying Ramp I #3
Qualifying Ramp Q #3
5
Winning Ramp I
Qualifying Ramp I #1
Qualifying Ramp I #2
Qualifying Ramp I #3
+
Final Ramp I
Winning Ramp Q
Qualifying Ramp Q #1
Qualifying Ramp Q #2
Qualifying Ramp Q #3
+
Final Ramp Q
To Flip/
Shift/QFTM
Logic

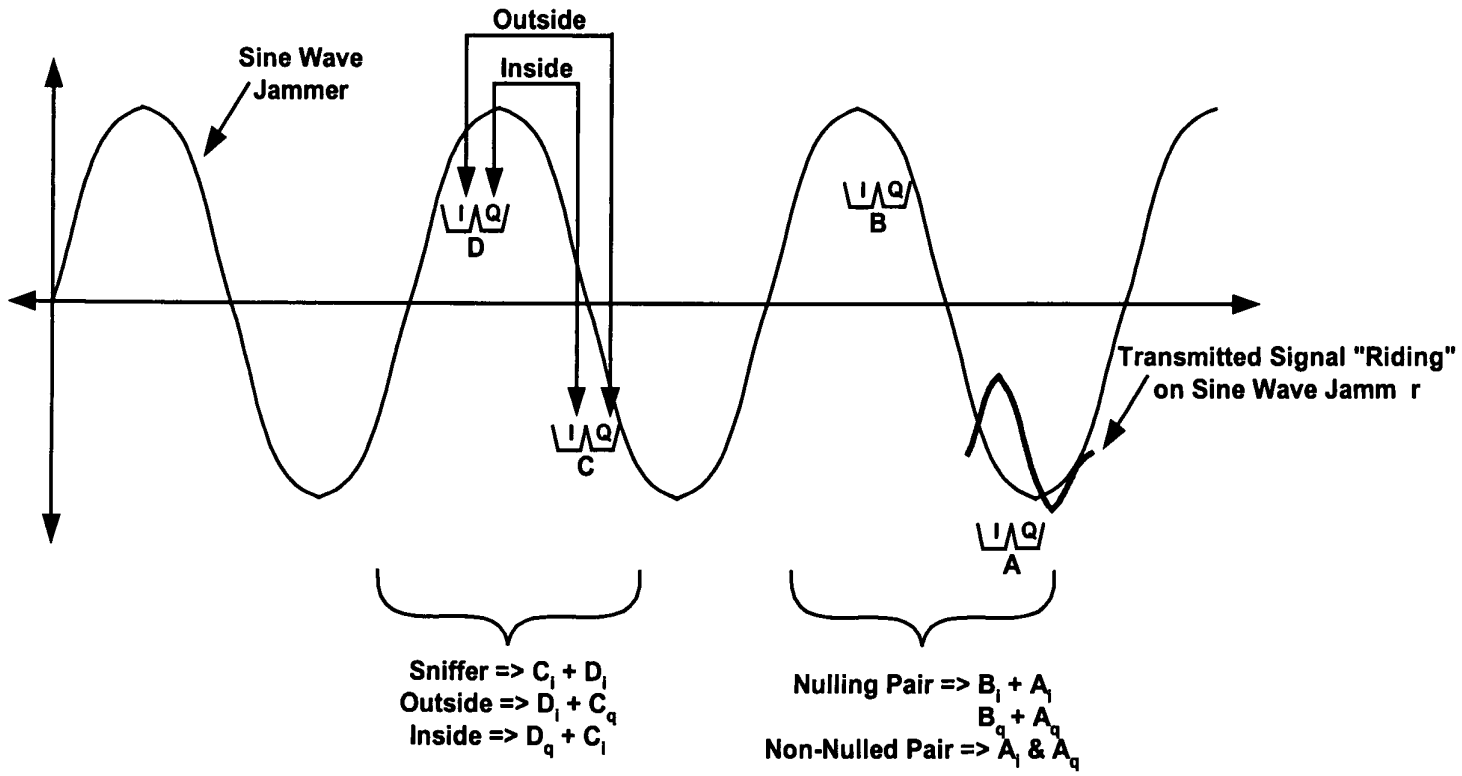
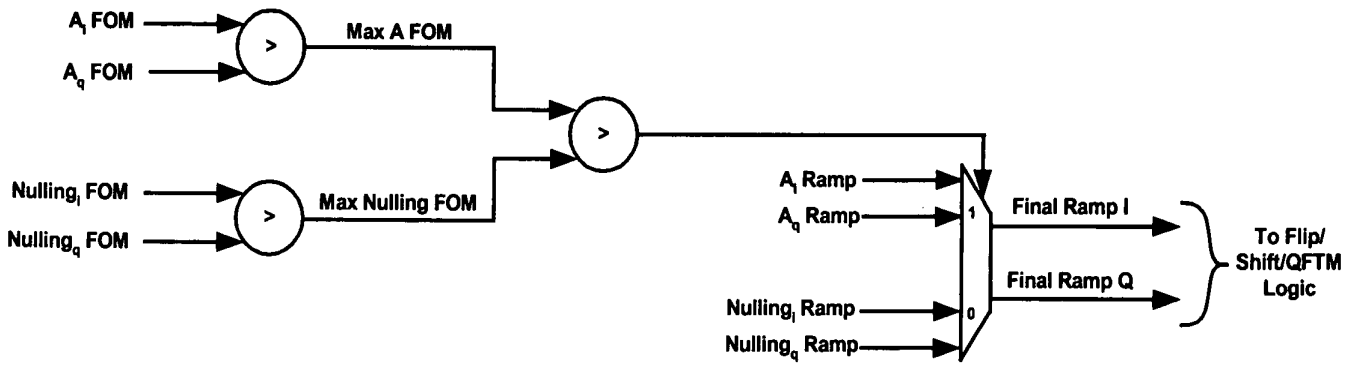

Outside
Inside
Sine Wave
Jammer
I Q
D
I Q
B
I Q
C
I Q
A
Transmitted Signal "Riding"
on Sine Wave Jamm r
Sniffer => $C_I + D_I$
Outside => $D_I + C_q$
Inside => $D_q + C_I$
Nulling Pair => $B_I + A_I$
$B_q + A_q$
Non-Nulled Pair => A_I & A_q

FIG. 63


A_I FOM
A_q FOM
>
Max A FOM
Nulling$_I$ FOM
Nulling$_q$ FOM
>
Max Nulling FOM
>
A_I Ramp
A_q Ramp
Nulling$_I$ Ramp
Nulling$_q$ Ramp
1
0
Final Ramp I
Final Ramp Q
To Flip/
Shift/QFTM
Logic

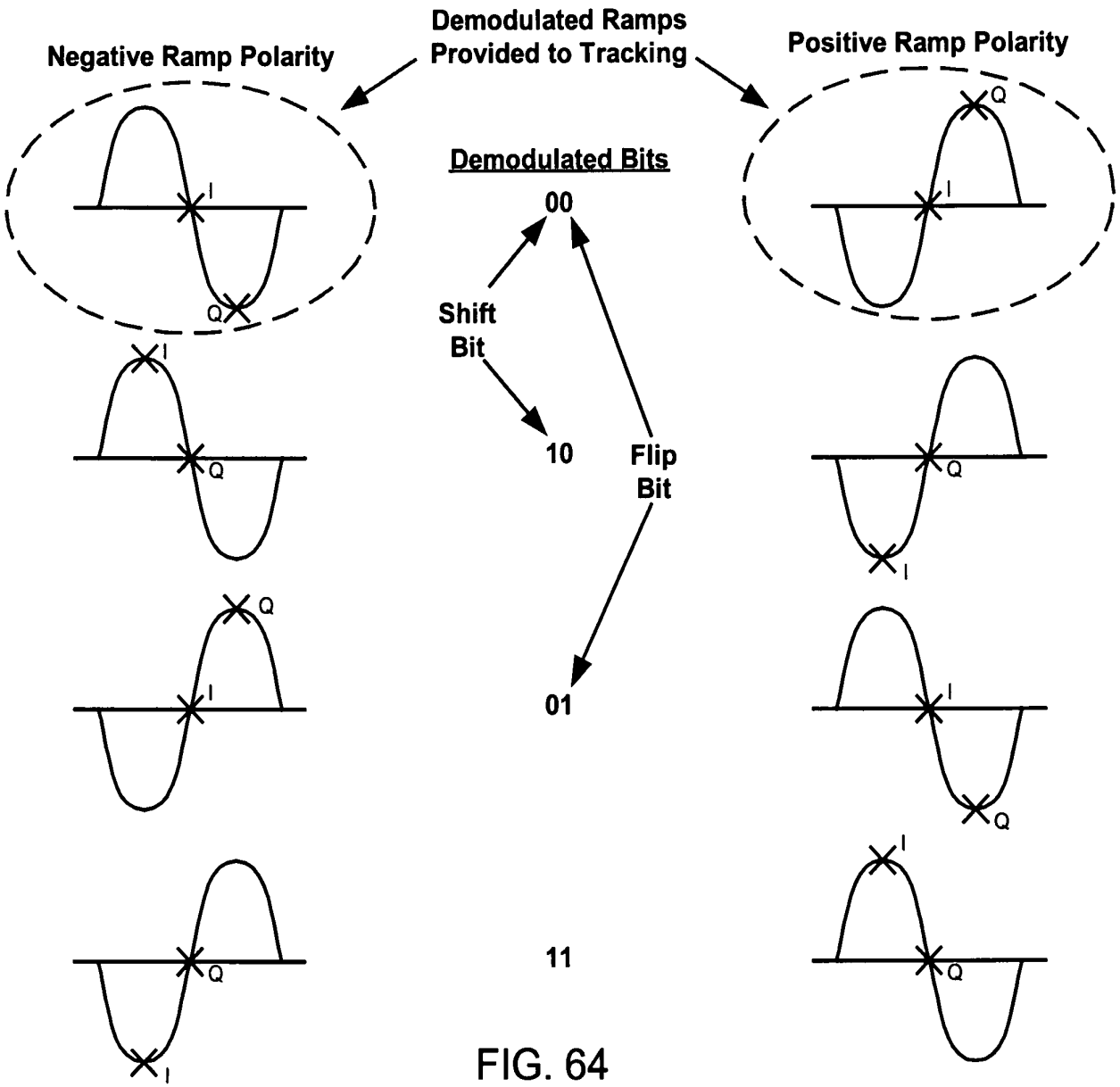

Demodulated Ramps
Provided to Tracking
Negative Ramp Polarity
Positive Ramp Polarity
Demodulated Bits
00
Shift
Bit
10
Flip
Bit
01
11
I
Q

FIG. 64

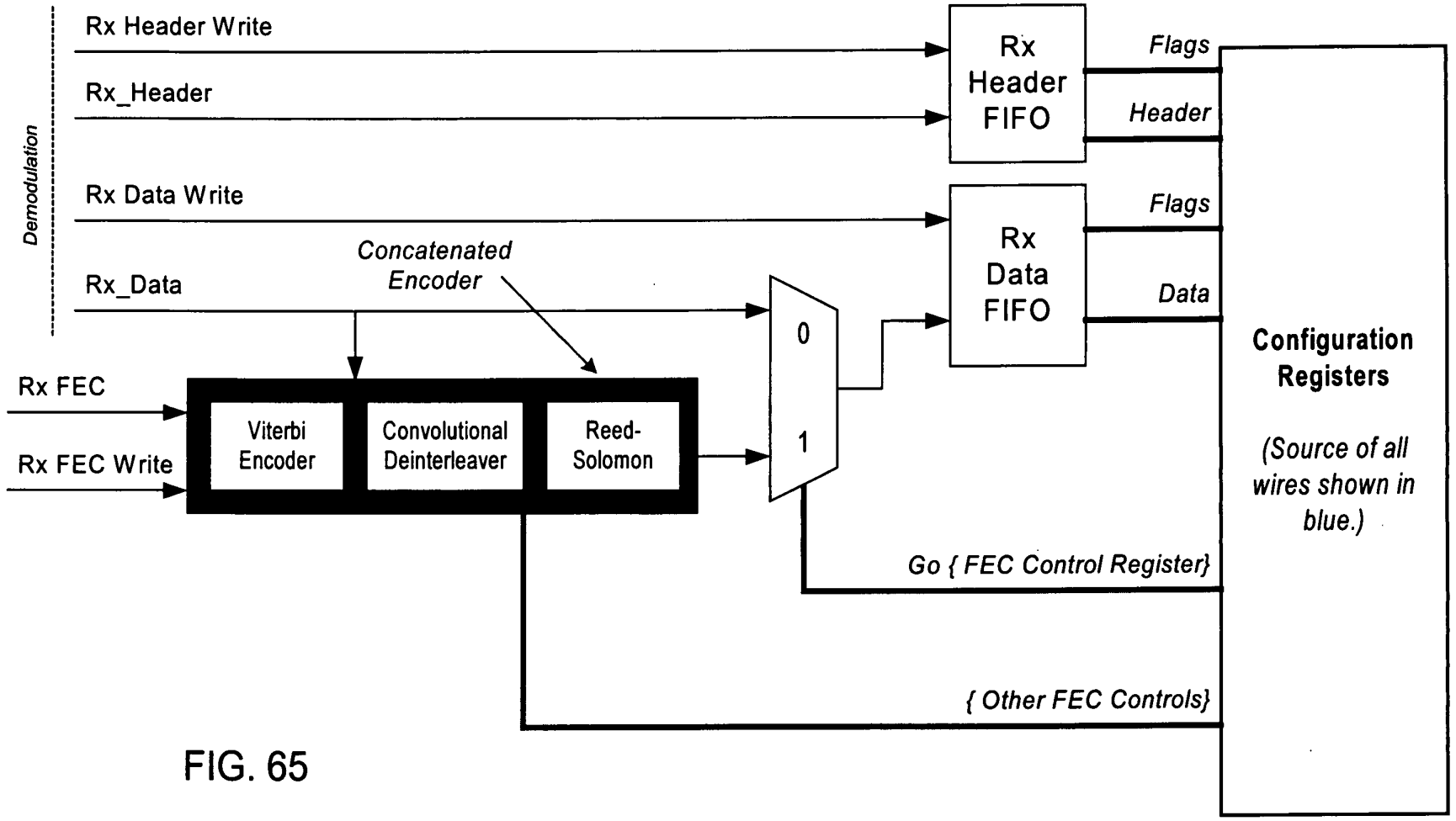

Demodulation
Rx Header Write
Rx_Header
Rx Data Write
Rx_Data
Concatenated Encoder
Rx FEC
Rx FEC Write
Viterbi Encoder
Convolutional Deinterleaver
Reed-Solomon
0
1
Rx Header FIFO
Rx Data FIFO
Flags
Header
Flags
Data
Configuration Registers
(Source of all wires shown in blue.)
Go { FEC Control Register}
{ Other FEC Controls}

FIG. 65

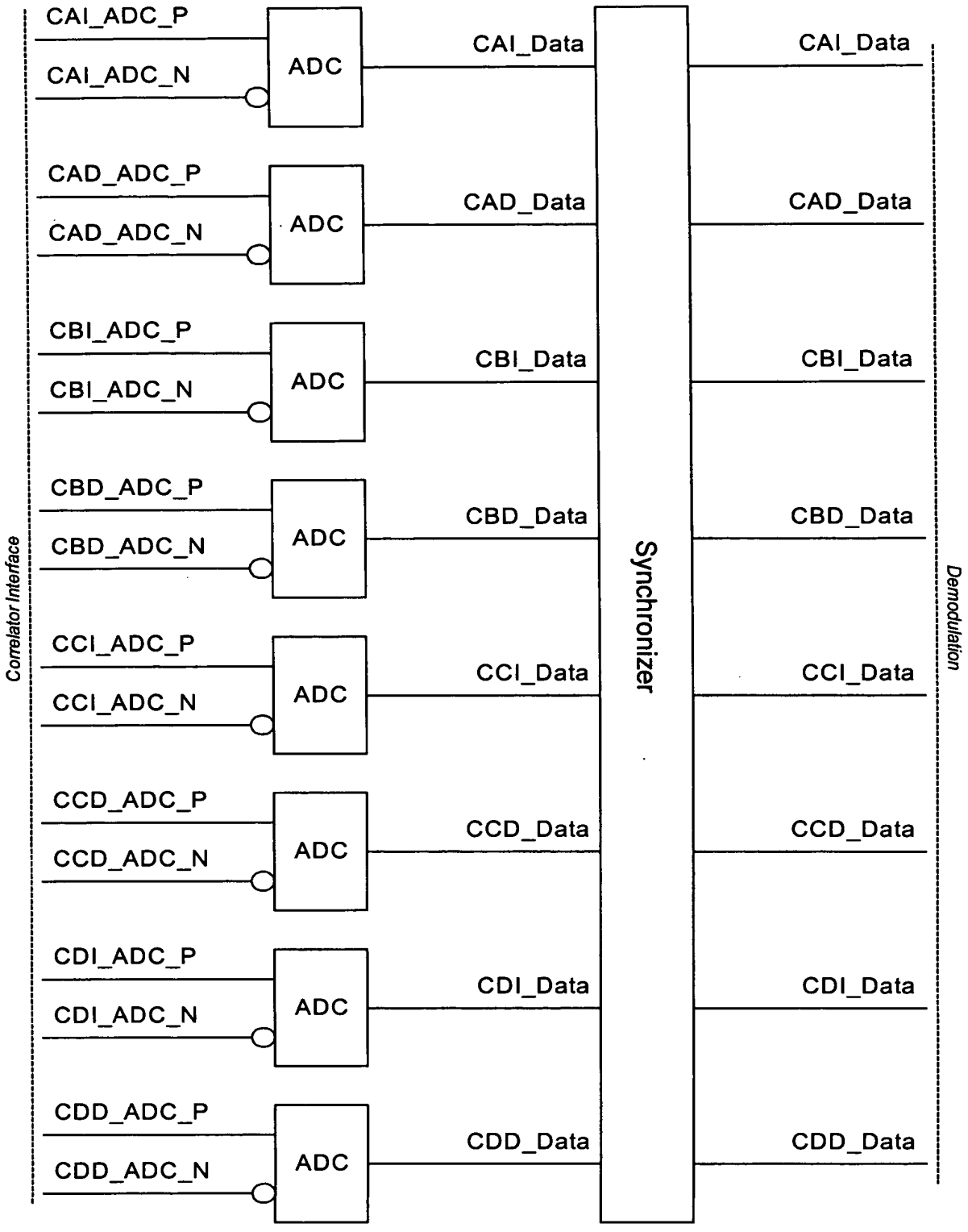

Correlator Interface
CAI_ADC_P
CAI_ADC_N
ADC
CAI_Data
CAD_ADC_P
CAD_ADC_N
ADC
CAD_Data
CBI_ADC_P
CBI_ADC_N
ADC
CBI_Data
CBD_ADC_P
CBD_ADC_N
ADC
CBD_Data
CCI_ADC_P
CCI_ADC_N
ADC
CCI_Data
CCD_ADC_P
CCD_ADC_N
ADC
CCD_Data
CDI_ADC_P
CDI_ADC_N
ADC
CDI_Data
CDD_ADC_P
CDD_ADC_N
ADC
CDD_Data
Synchronizer
CAI_Data
CAD_Data
CBI_Data
CBD_Data
CCI_Data
CCD_Data
CDI_Data
CDD_Data
Demodulation

FIG. 66

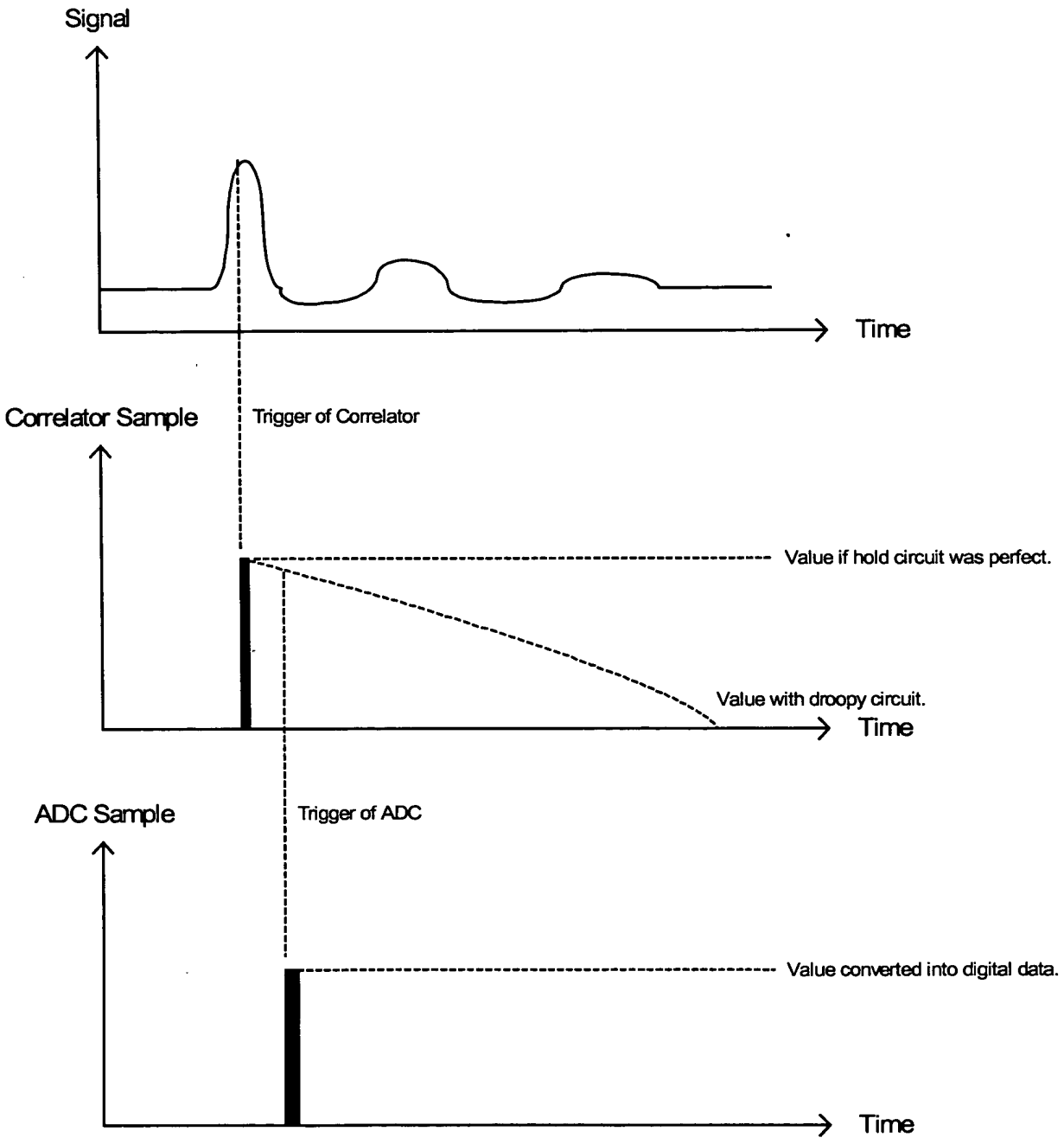
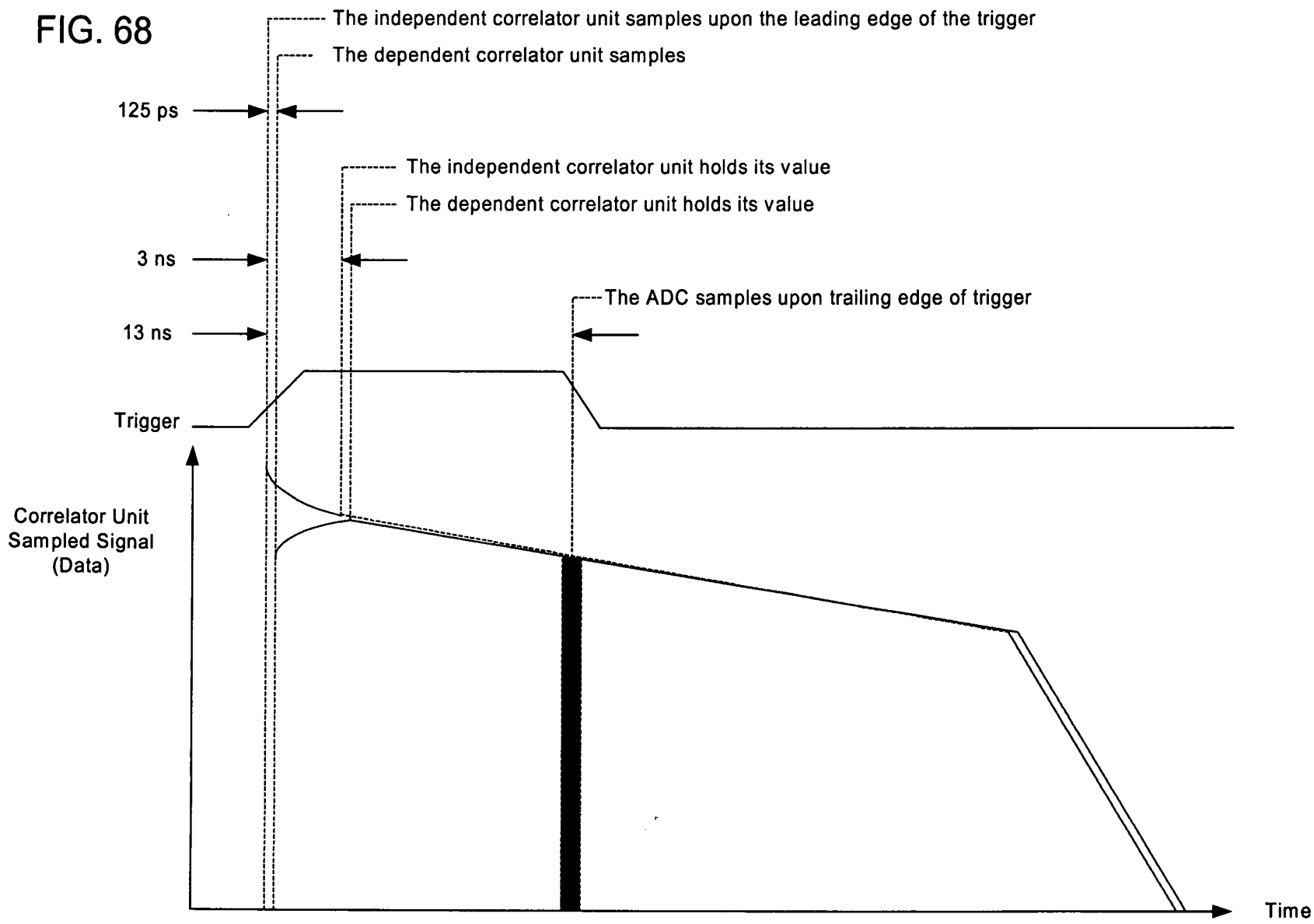

Signal
Time
Correlator Sample
Trigger of Correlator
Value if hold circuit was perfect.
Value with droopy circuit.
Time
ADC Sample
Trigger of ADC
Value converted into digital data.
Time

FIG. 67

FIG. 68


The independent correlator unit samples upon the leading edge of the trigger
The dependent correlator unit samples
125 ps
The independent correlator unit holds its value
The dependent correlator unit holds its value
3 ns
The ADC samples upon trailing edge of trigger
13 ns
Trigger
Correlator Unit
Sampled Signal
(Data)
Time

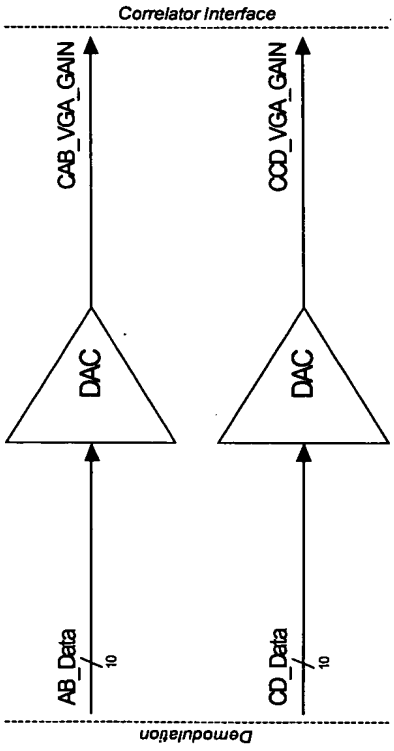

Correlator Interface
CAB_VGA_GAIN
CCD_VGA_GAIN
DAC
DAC
AB_Data
10
CD_Data
10
Demodulation

FIG. 69